COMPAL CONFIDENTIAL

MODEL NAME :DDM70

PCB NO : LA-F402P

BOM P/N : 431A8F31LXX

BR MLK14 KBL-U UMA

KABYLAKE-U42

2018-08-17

REV :1.0 (A00)

@ : Nopop Component
EMC@ : EMI, ESD and RF Component
@EMC@ : EMI, ESD and
RF Nopop Component CXDP
@ : XDP Component
CONN@ : Connector Component
U42@ : KBL-R U42 Component
U22@ : KBL-R U22 Component
DS3@ : Support DS3 Component
NDS3@ : No Support DS3 Component
650@ : Pop NPCT650VB2YX Component
750@ : Pop NPCT750JAAYX Component

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

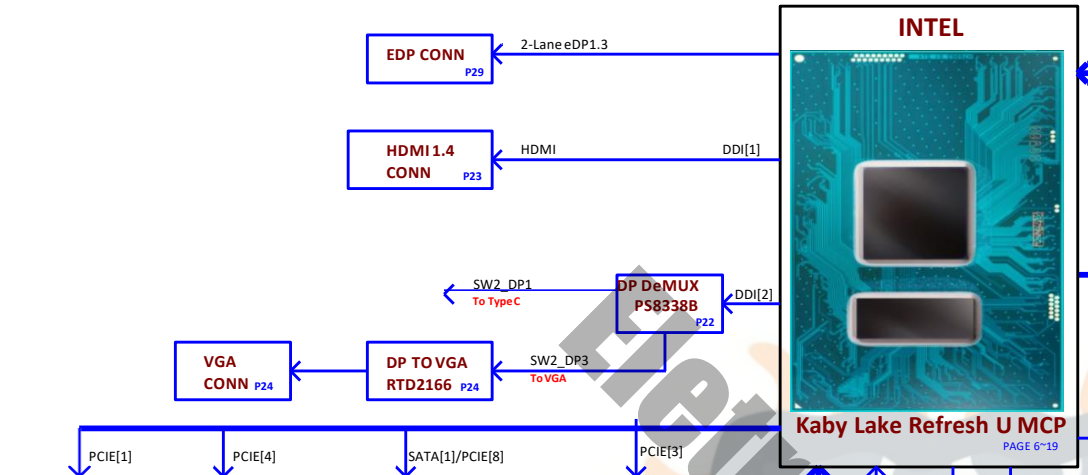
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title	Cover Sheet	
Size	Document Number: LA-F402P	Rev: 1.0
Date: Friday, August 17, 2018	Sheet 1 of 82	

Eletro-X Technical

BreckenridgeMLK 14 UMA Block Diagram



Reverse Type

Memory BUS (DDR4)
DDR4 2133MHz for KBL-U
DDR4 2400MHz for KBL-H
Up to 2x8GB Modules

DDR4-SO-DIMM X2
BANK 0, 1, 2, 3
P20~21

EDP CONN P29 — 2-Lane eDP1.3

HDMI 1.4 CONN P23 — HDMI — DDI[1]

DP DeMUX PS8338B P22 — DDI[2]
SW2_DP1 To Type C

VGA CONN P24
DP TO VGA RTD2166 P24 — SW2_DP3 To VGA

USB

USB2.0[8] LCD Touch P29
USB2.0[5] Camera P29
Trough eDP Cable

USB2.0[9] SLGC55544BVTR USB POWER SHARE P43 — USB2.0[9]_PS
USB3.0[6] USB3 Repeater PS8713B P42 — USB3.0[6]
USB3.0 Conn PS(Ext Port 1) P43

USB2.0[2] USB3.0 Conn (Ext Port 2) P44
USB3.0[3]
USB2.0[3] USB3.0 Conn (Ext Port 3) P44
USB3.0[4]

PCIE[1] Card reader RTS5242 P31 — SD4.0 P31
PCIE[4] Intel Jacksonville WGI219LM P30 — Transformer P30 — RJ45 P30
SATA[1]/PCIE[8] SATA/PCIE REPEATER PS8558 x1 P32 — SATA[1]/PCIE[8] M.2,3042 Key B WWAN/LTE/HCA P33 — USB2.0[4] — USB3.0[2]
PCIE[3] M.2,3030 Key A WLAN+BT P33 — USB2.0[7]

SATA[0]
SATA[2]/PCIE[12][11]
HD Audio I/F
HDA Codec ALC3246 P34
INT.Speaker P34
Universal Jack P34
Dig. MIC P29
Trough eDP Cable

SPI
ESPI
W25Q128JVSIQ P8
128M 4K sector
W25Q128JVSIQ P8
128M 4K sector reserve
TPM1.2/2.0 Nuvoton NPCT750JAAYX P39

SMSC KBC MEC5105 P35-36
KB/TP CONN P45
FAN CONN P36

SATA REPEATER PI3EQX6741STZDEX P41
SATA HDD Conn P41
SATA/PCIE REPEATER PS8558 x2 P39
M.2 2280 SSD Conn P40

LID SWITCH LED board P46
USH CONN P38
CPU&PCH XDP Port P14
AUTOMATIC POWER SWITCH(APS) P11
Free Fall sensor P41
DC/DC Interface P47
POWER ON/OFF SW & LED P46

Non-AR Type C

USB 3.0 + AM Type C CONN. P28
TX/RX — HS Redriver Switch TUSB546@ PS8743@ P25 — DP1.2 4 lanes — SW2_DP1, USB3.0[1]
GPIO
USB2.0 — PD Solution TPS65982DC P26-27 — SMBUS, USB2.0[1]
CC
Vbus
5V VR
Charger

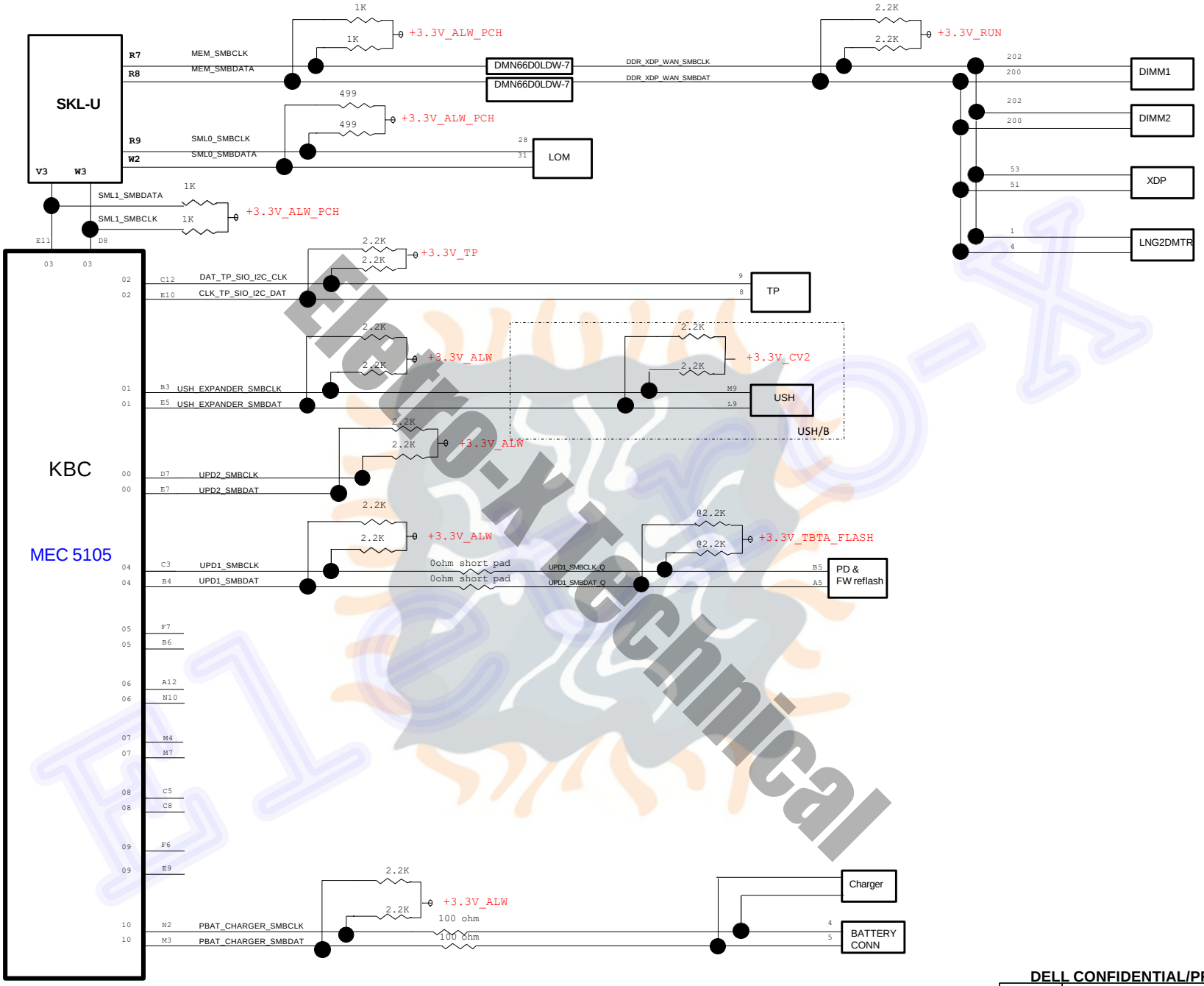
Smart Card — TDA8034HN — USH TPM1.2 BCM58102 P39 — USB2.0[10]
RFID/NFC — SPI
Fingerprint CONN — SPI
USH board P39

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL"). THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.
Title: Block diagram
Size: Document Number: LA-F402P
Date: Friday, August 17, 2018 Sheet 2

Eletro-X Technical



Eletro-X Technical

DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.

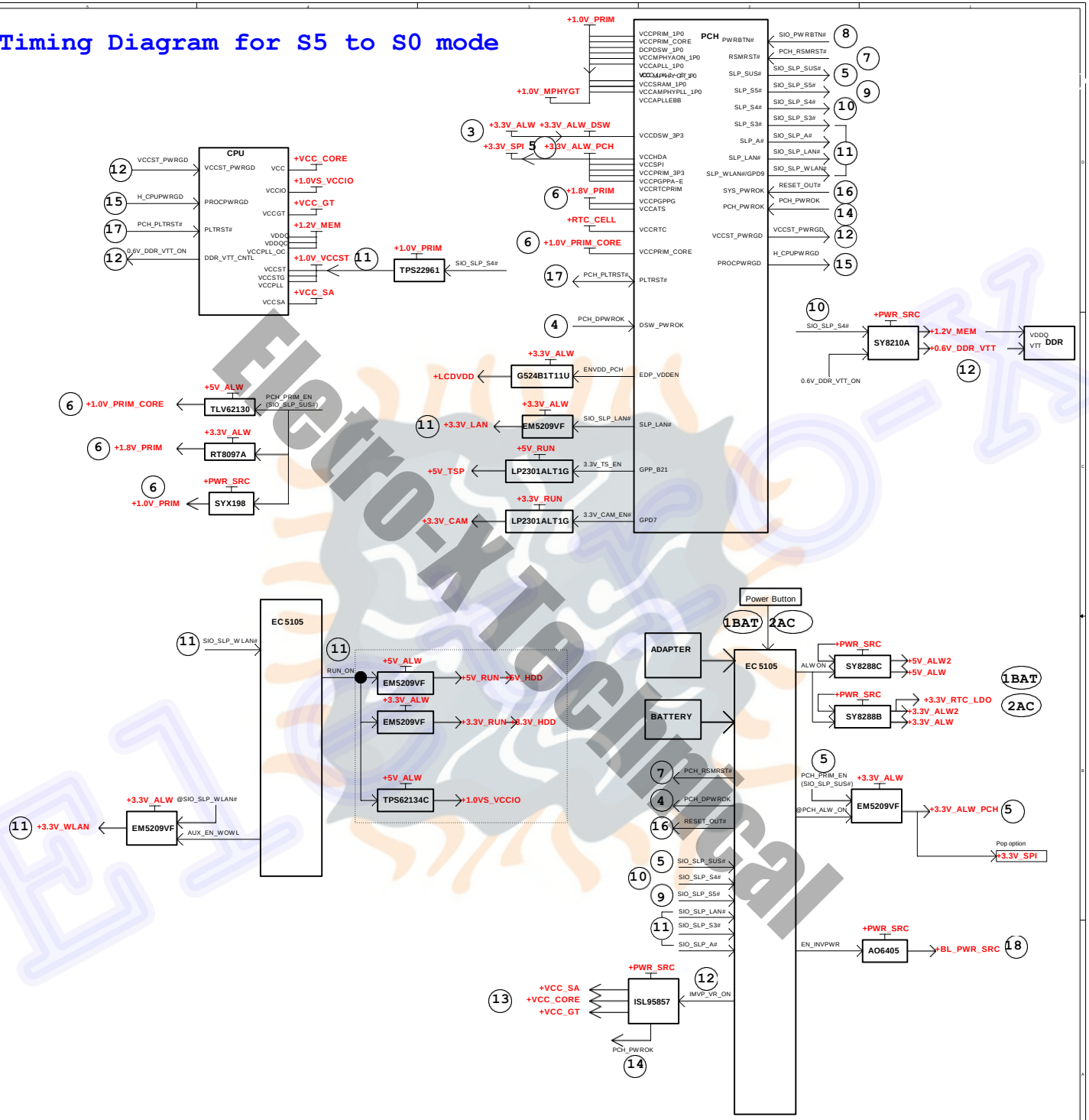
Title: Port assignment

Size: Document Number: LA-F402P

Date: Friday, August 17, 2018 Sheet 5

Eletro-X

Timing Diagram for S5 to S0 mode



Electro-X Technical

DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL"). THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.

Power Sequence

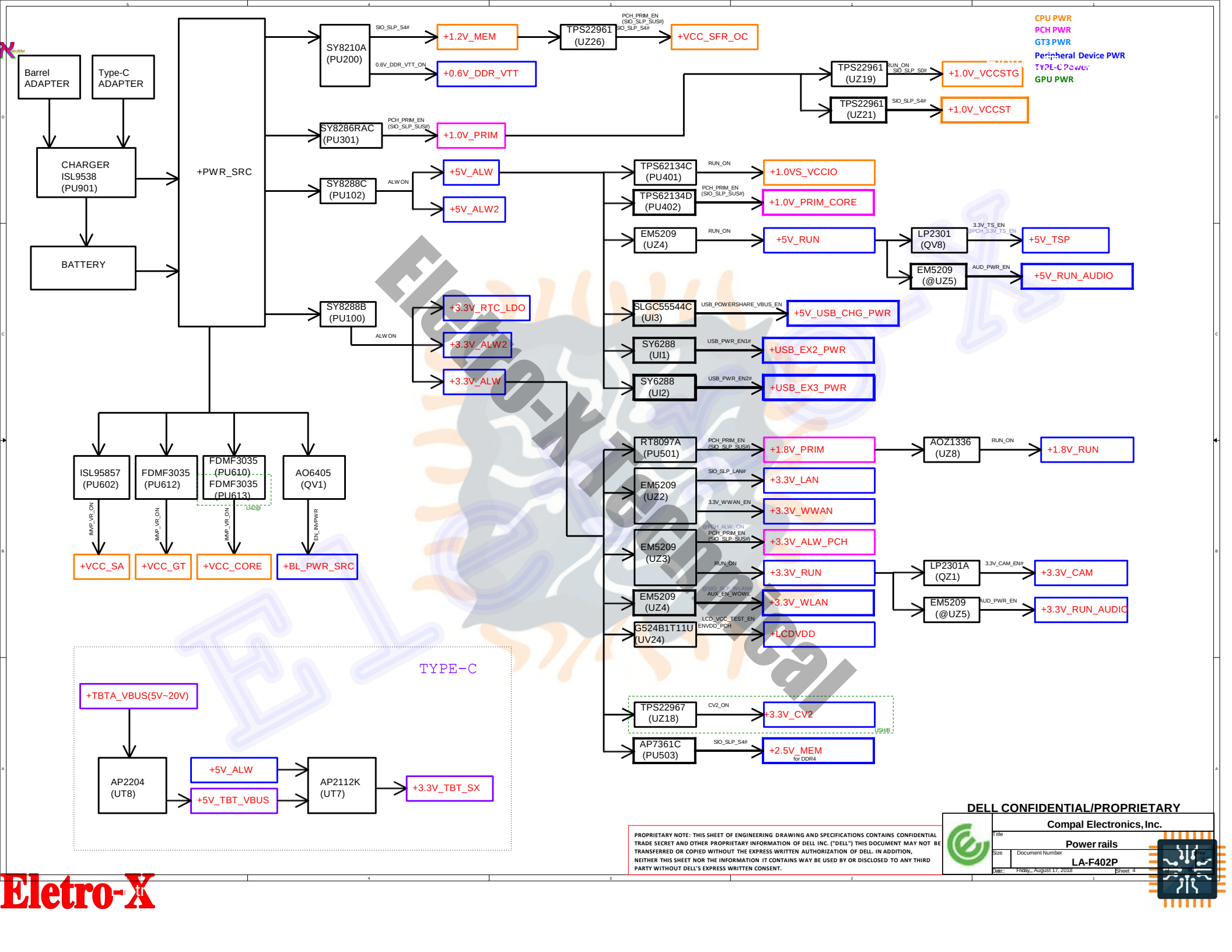
LA-F402P

Rev 0.2

Date: Friday, August 17, 2018

Sheet 46 of 69

Eletro-X



Eletro-X Technical

DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.

Title: Power rails

Size: | Document Number: LA-F402P | Rev:

Date: Friday, August 17, 2018 | Sheet 4

Eletro-X

For Breckenridge12/14/15 UMA

POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State \ power plane	+5V_ALW +3.3V_ALW +3.3V_ALW_DSW +3.3V_ALW_PCH +RTC_CELL +1.8V_PRIM +1.0V_PRIM +1.0V_PRIM_CORE +5V_ALW2 +3.3V_ALW2 +3.3V_RTC_LDO +1.0V_MPHYGT		
S0	ON	+3.3V_CV2 +1.2V_MEM +2.5V_MEM +1.0V_VCCST	+5V_RUN +3.3V_RUN +0.6V_DDR_VTT +1.8V_RUN +VCC_CORE +VCC_GT +VCC_SA +1.0VS_VCCIO
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF

USB3.0	SSIC	PCIE	SATA	DESTINATION
USB3.0-1				Type-C Port
USB3.0-2	SSIC			M.2 3042(LTE)
USB3.0-3				JUSB2-->Left
USB3.0-4				JUSB3-->Rear Left
USB3.0-5		PCIE-1		Card Reader
USB3.0-6		PCIE-2		JUSB1-->Right
		PCIE-3		M.2 3030(WLAN)
		PCIE-4		LOM
		PCIE-5		NA
		PCIE-6		NA
		PCIE-7	SATA-0	SATA HDD
		PCIE-8	SATA-1	M.2 3042(SATA Cache or HCA)
		PCIE-9		NA
		PCIE-10		NA
		PCIE-11	SATA-1*	M.2 2280 SSD (PCIex2 or SATA)
		PCIE-12	SATA-2	

12" not support JUSB3

USB PORT#	DESTINATION
1	Type-C Port
2	JUSB2-->Left
3	JUSB3-->Rear Left
4	M2 3042(WWAN)
5	Camera
6	NA
7	M.2 3030(BT)
8	Touch Screen
9	JUSB1-->Right
10	USH

Eletro-X Technical

DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.

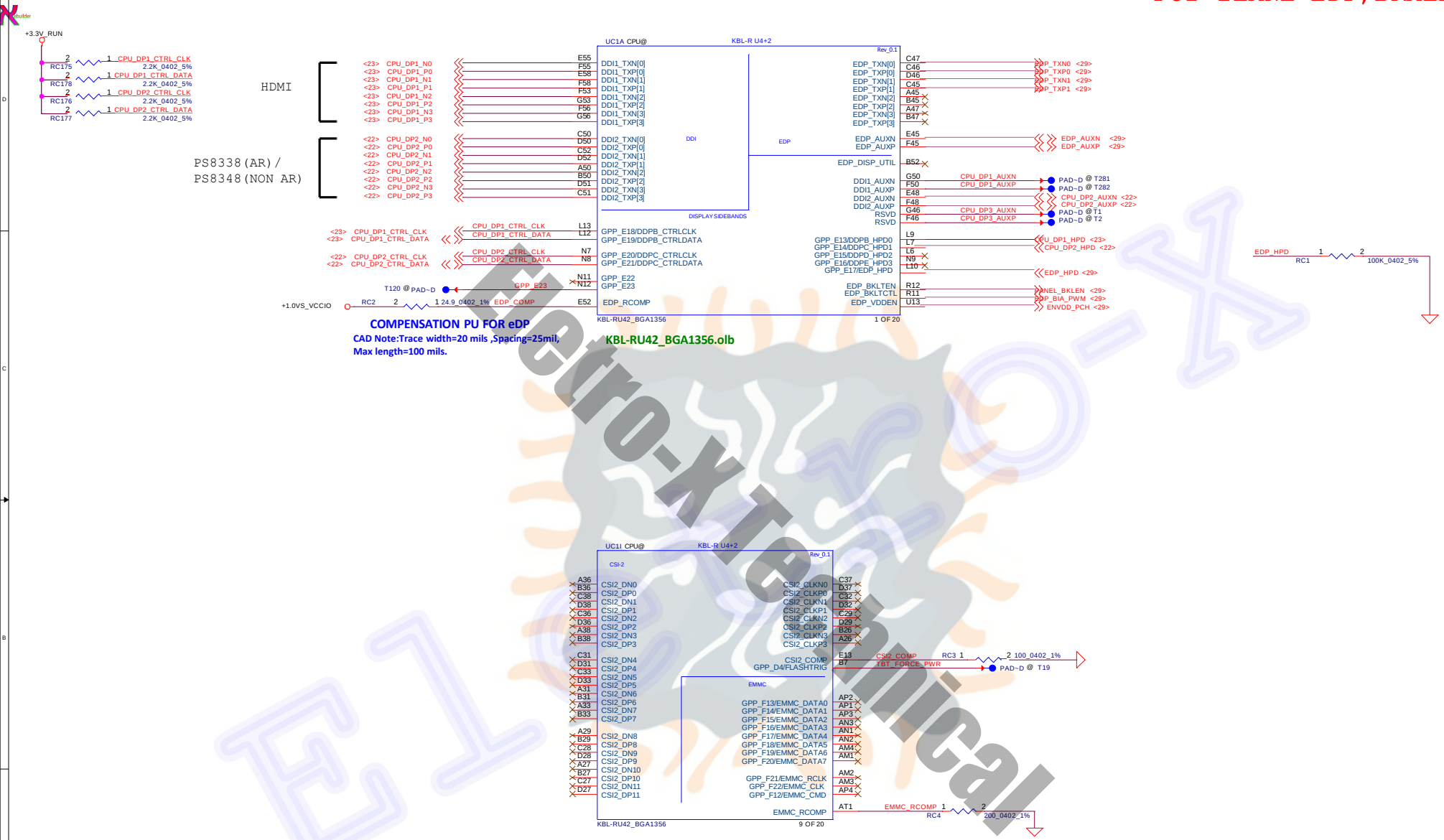
Title: Port assignment

Size: | Document Number: LA-F402P | Rev:

Date: Friday, August 17, 2018 | Sheet 3

Eletro-X

For 2LANE EDP,BRMLK12



Eletro-X Technical

DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

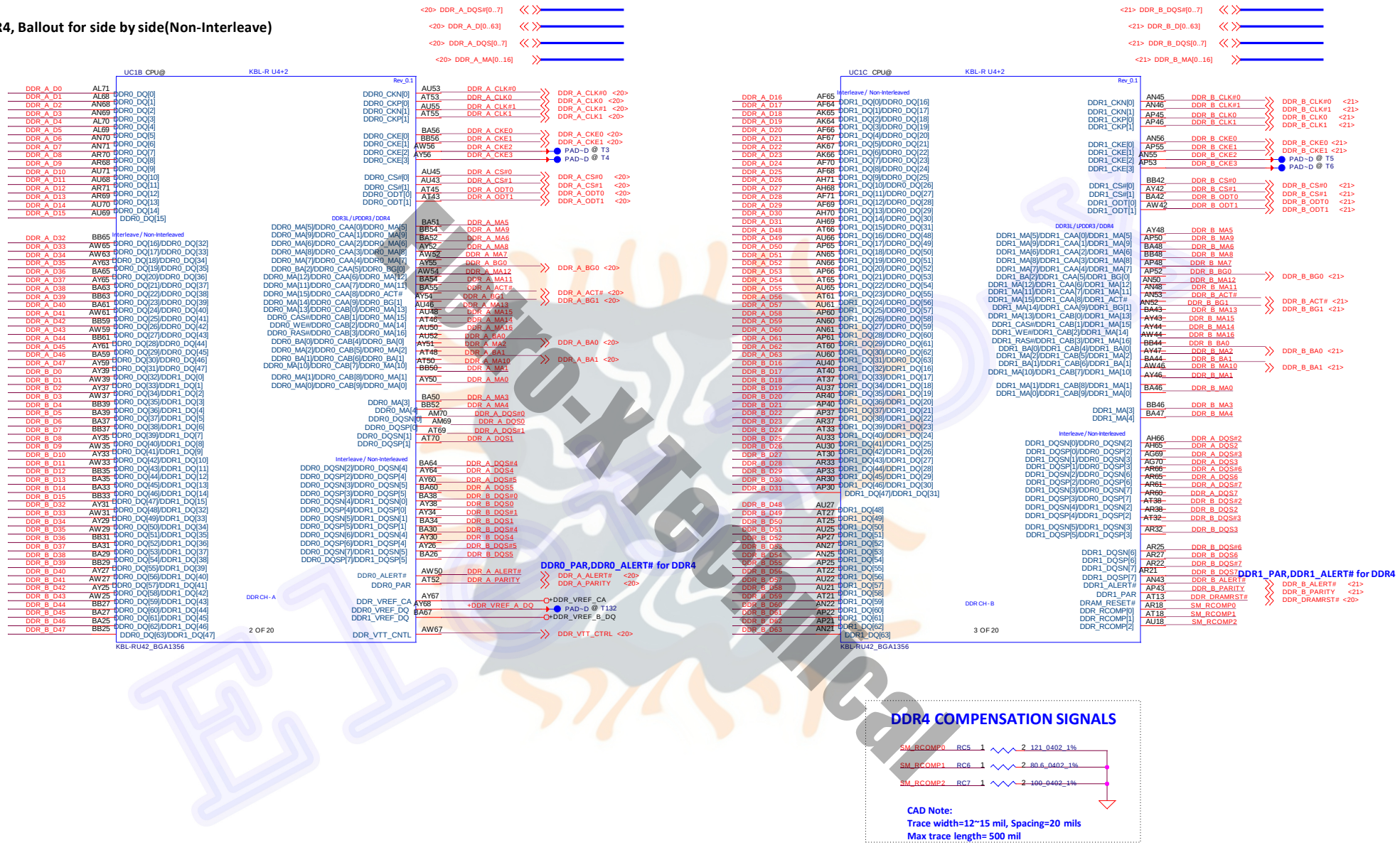
Compal Electronics, Inc.

Title	CPU (1/14)	
Size	Document Number	Rev
	LA-F402P	
Date: Friday, August 17, 2018	Sheet 6	

Eletro-X

For DDR4

DDR4, Ballot for side by side(Non-Interleave)



DDR4 COMPENSATION SIGNALS

CAD Note:
Trace width=12~15 mil, Spacing=20 mils
Max trace length= 500 mil

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title	CPU (2/14)	
Size	Document Number	Rev
	LA-F402P	
Date:	Friday, August 17, 2018	Sheet 7

Eletro-X Technical

SPI_MOSI= SPI_IO0
SPI_MISO= SPI_IO1
PCH EDS R0.7 p.235~236

For BR/SB

SOFTWARE TAA

128Mb Flash ROM

128Mb Flash ROM

RF Request

Place close CPU side

TLS CONFIDENTIALITY

HIGH	ENABLE
LOW(DEFAULT)	DISABLE

WEAK INTERNAL 20K PD

EC interface

HIGH	ESPI
LOW(DEFAULT)	LPC

WEAK INTERNAL 20k PD

EXI BOOT STALL BYPASS

HIGH	ENABLED
LOW(DEFAULT)	DIABLED

WEAK INTERNAL PD

Eletro-X Technology

DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.

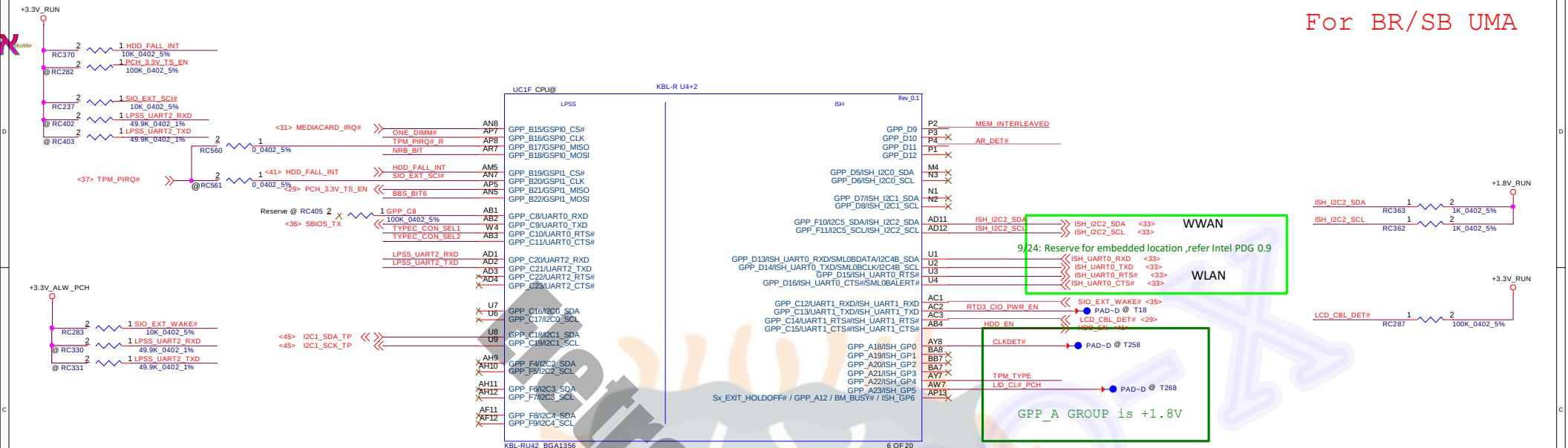
Title: CPU (3/14)

Size: | Document Number: LA-F402P | Rev:

Date: Friday, August 17, 2018 | Sheet 8

Eletro-X

For BR/SB UMA

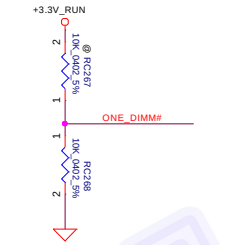


NO REBOOT STRAP	
HIGH	No REBOOT
LOW(DEFAULT)	REBOOT ENABLE

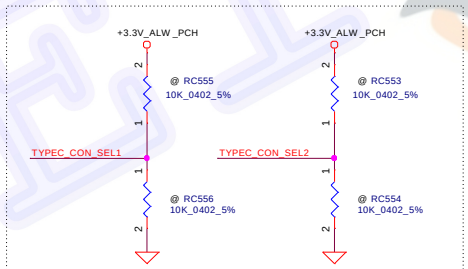
Internal 20k PD

BOOT BIOS Destination(Bit 6)	
HIGH	LPC
LOW(DEFAULT)	SPI

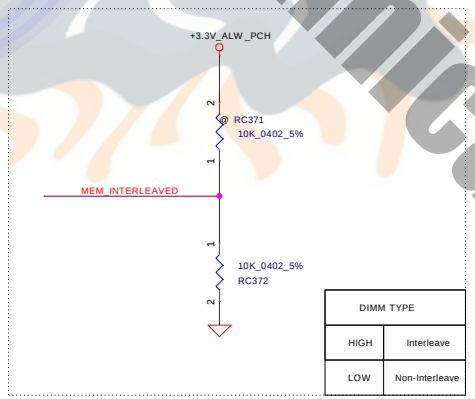
Internal 20k PD



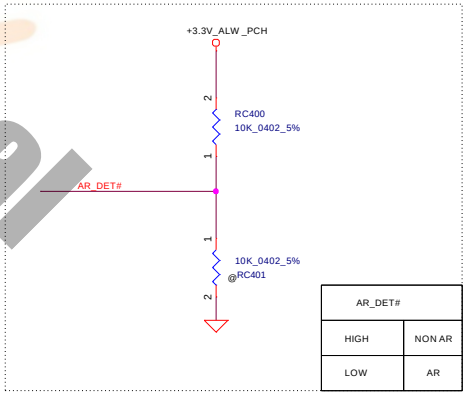
DIMM Detect	
HIGH	1 DIMM
LOW	2 DIMM



Vendor	JAE	FOXCON	TBD	TBD
TYPEC_CON_SEL1	LOW	LOW	HIGH	HIGH
TYPEC_CON_SEL2	LOW	HIGH	LOW	HIGH



DIMM TYPE	
HIGH	Interleave
LOW	Non-Interleave



AR_DET#	
HIGH	NON AR
LOW	AR

DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.

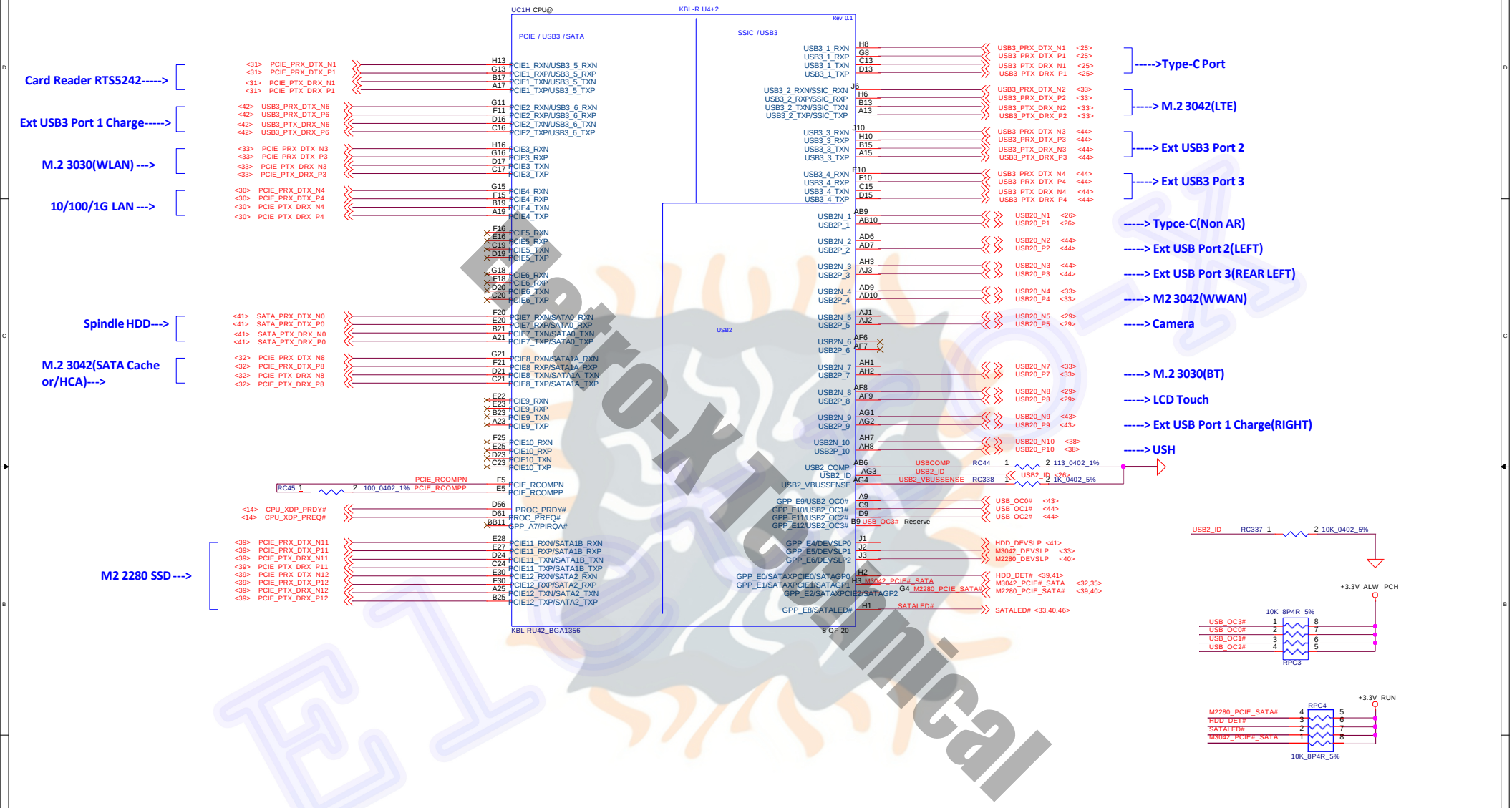
Title: CPU (4/14)

Size: | Document Number: LA-F402P

Date: Friday, August 17, 2018 | Sheet 9

Eletro-X Technical

For NON AR, Breckenridge 12/14/15 UMA



Eletro-X Technical

DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.

Title	CPU (5/14)	
Size	Document Number	Rev
	LA-F402P	
Date:	Friday, August 17, 2018	Sheet 10

Eletro-X

For BR UMA

For KBL-R U22

For KBL-R U42

WWAN--->

WLAN--->

M.2 SDD--->

LAN--->

Card Reader --->

MLCC downsize 4/18

CMOS1 must take care short & touch risk on layout placement

	RC439	RC440	RE536	RC215	RC441	RC442
Support DS3	V	X	V	X	V	X
No Support DS3	X	V	X	V	X	V

'V' mean POP, 'X' mean DEPOP

RC215	
POP DE-POP	NO Support Deep sleep Support Deep sleep

if pop UC12, RC291 also need pop(74AHC1G09GW is OD output)

Eletro-X Technical

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

DELL CONFIDENTIAL/PROPRIETARY

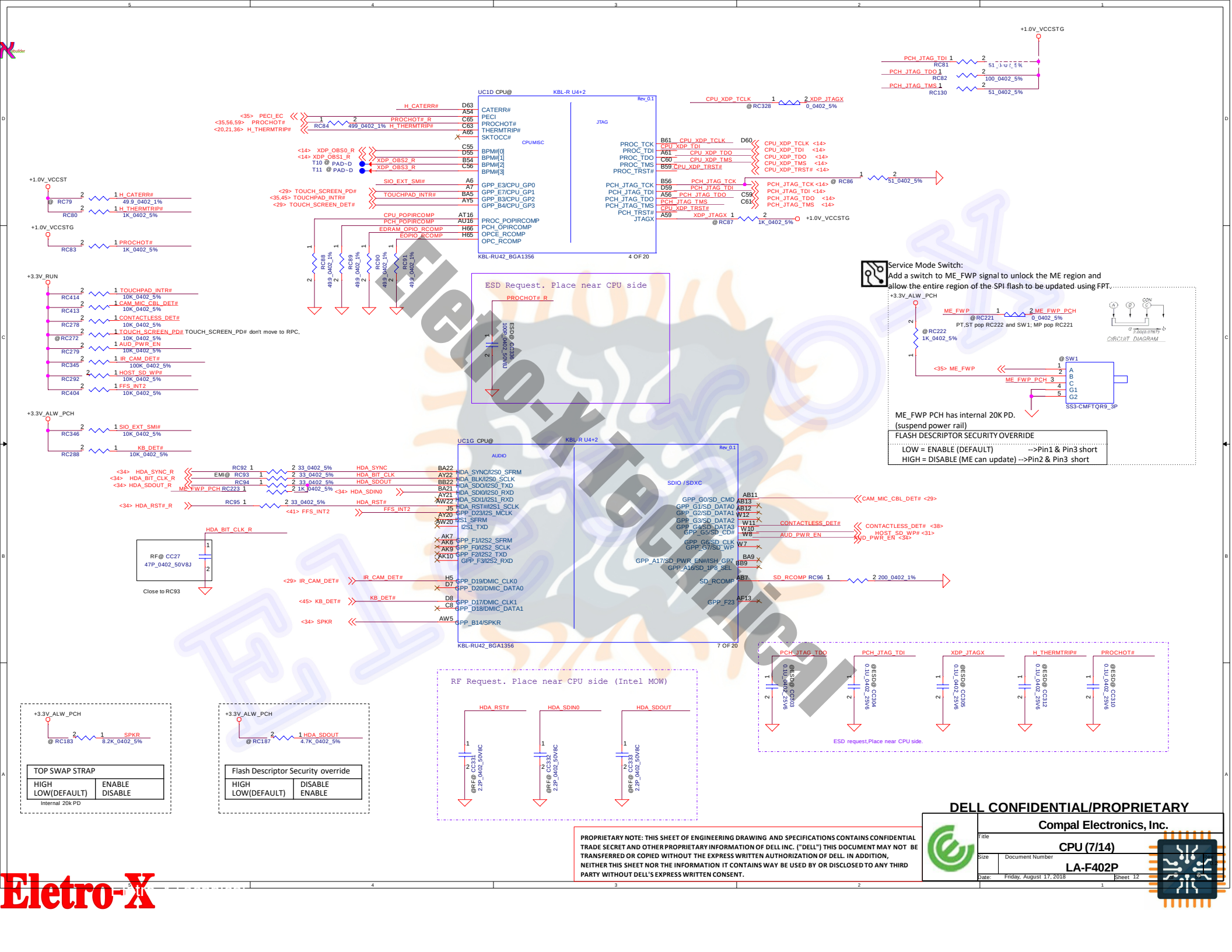
Compal Electronics, Inc.

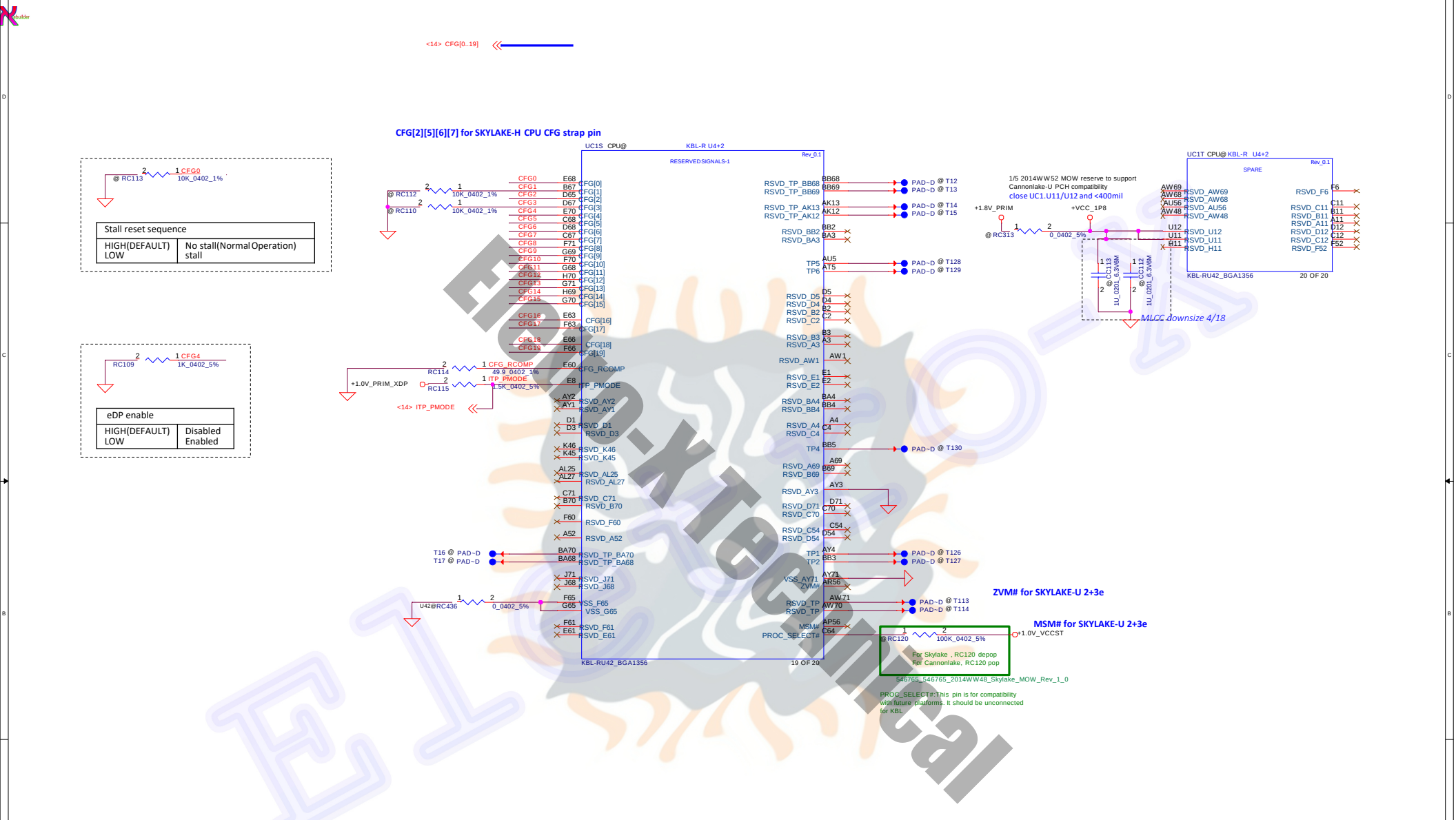
Title: CPU (6/14)

Size: | Document Number: LA-F402P

Date: Friday, August 17, 2018 | Sheet 11

Eletro-X


UC1D CPU@
KBL-R U4+2
KBL-RU42_BGA1356
4 OF 20
UC1G CPU@
KBL-R U4+2
KBL-RU42_BGA1356
7 OF 20
ESD Request. Place near CPU side
Service Mode Switch:
Add a switch to ME_FWP signal to unlock the ME region and allow the entire region of the SPI flash to be updated using FPT.
ME_FWP PCH has internal 20K PD. (suspend power rail)
FLASH DESCRIPTOR SECURITY OVERRIDE
LOW = ENABLE (DEFAULT) -->Pin1 & Pin3 short
HIGH = DISABLE (ME can update) -->Pin2 & Pin3 short
TOP SWAP STRAP
HIGH ENABLE
LOW(DEFAULT) DISABLE
Internal 20k PD
Flash Descriptor Security override
HIGH DISABLE
LOW(DEFAULT) ENABLE
RF Request. Place near CPU side (Intel MOW)
ESD request,Place near CPU side.
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
CPU (7/14)
LA-F402P
Friday, August 17, 2018
Sheet 12
PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.



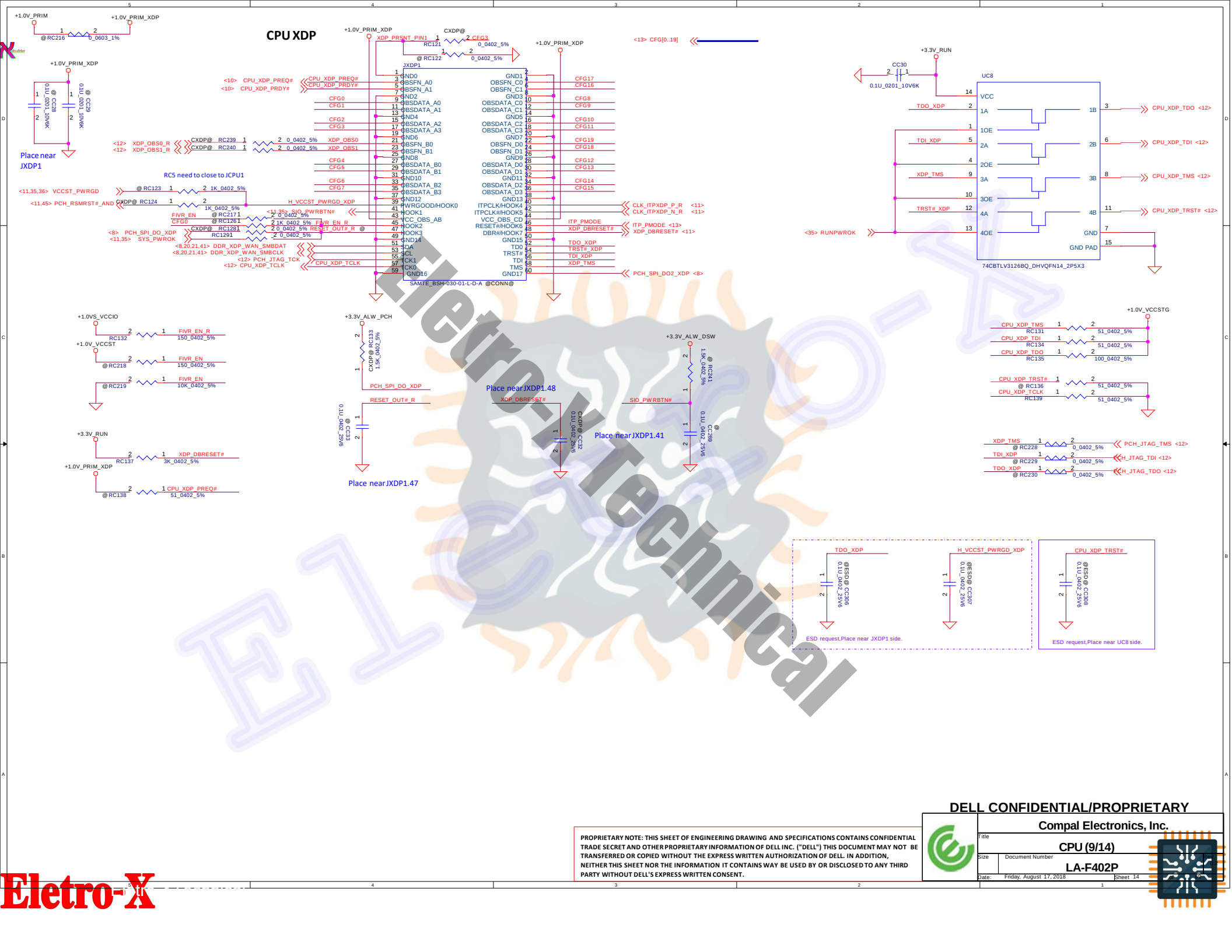
PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title	CPU (8/14)	
Size	Document Number	Rev
	LA-F402P	
Date: Friday, August 17, 2018	Sheet 13	

Eletro-X Technical



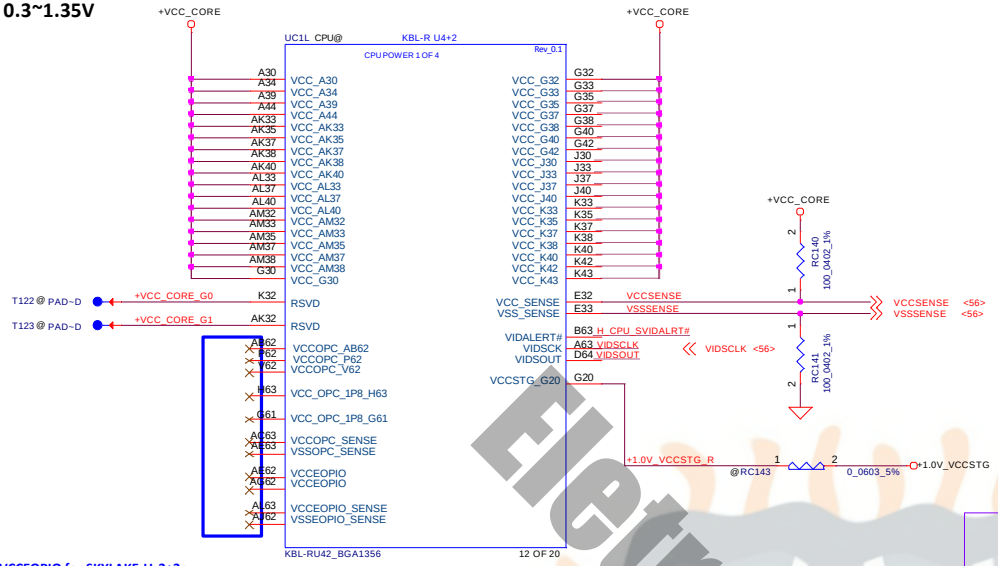
DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN addition, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

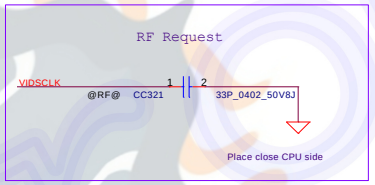
Compal Electronics, Inc.

Title	CPU (9/14)	
Size	Document Number	Rev
	LA-F402P	
Date: Friday, August 17, 2018	Sheet 14	

+VCC_CORE: 0.3~1.35V

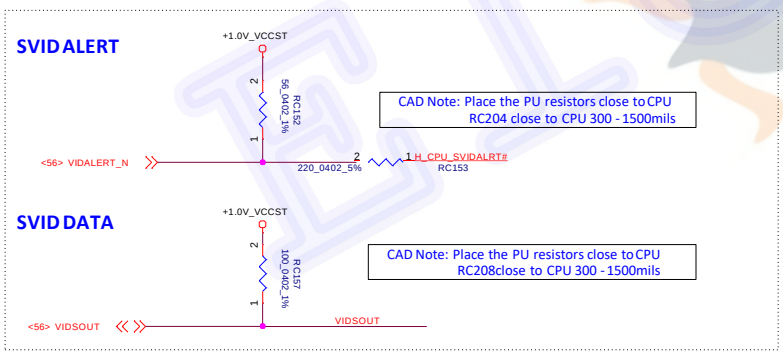


VCCOPC,VCCOPC_1P8,VCCEOPIO for SKYLAKE-U 2+3e
(w/ on package cache)



PSC(Primary side cap) : Place as close to the package as possible
BSC(Backside cap) : Place on secondary side, underneath the package

Component placement order:
Package edge > 0402 caps > 0805 caps > Bulk caps >Power source



Eletro-X Technical

DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.

Title: CPU (10/14)

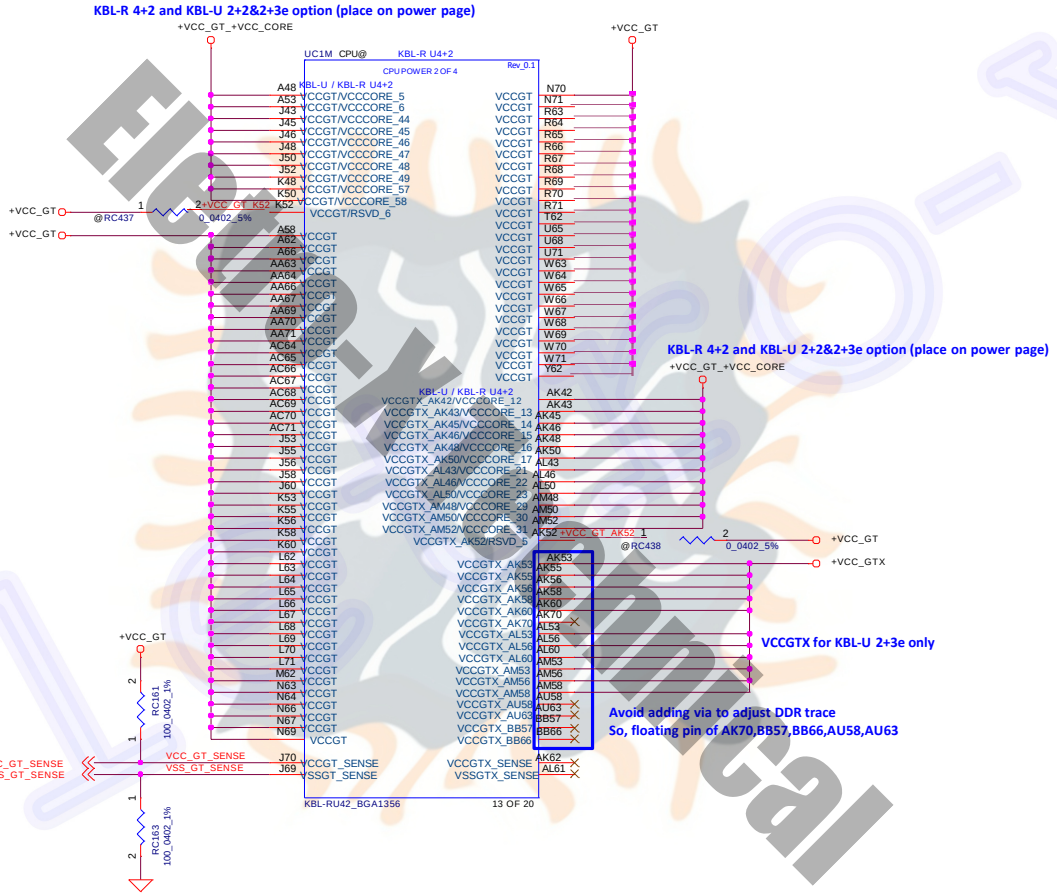
Size: | Document Number: LA-F402P

Date: Friday, August 17, 2018 | Sheet 15

Eletro-X

Follow KBL-R_U42_Processor_Line_BGA1356_Ballout_Rev1p0

+VCCGT: 0.3~1.35V



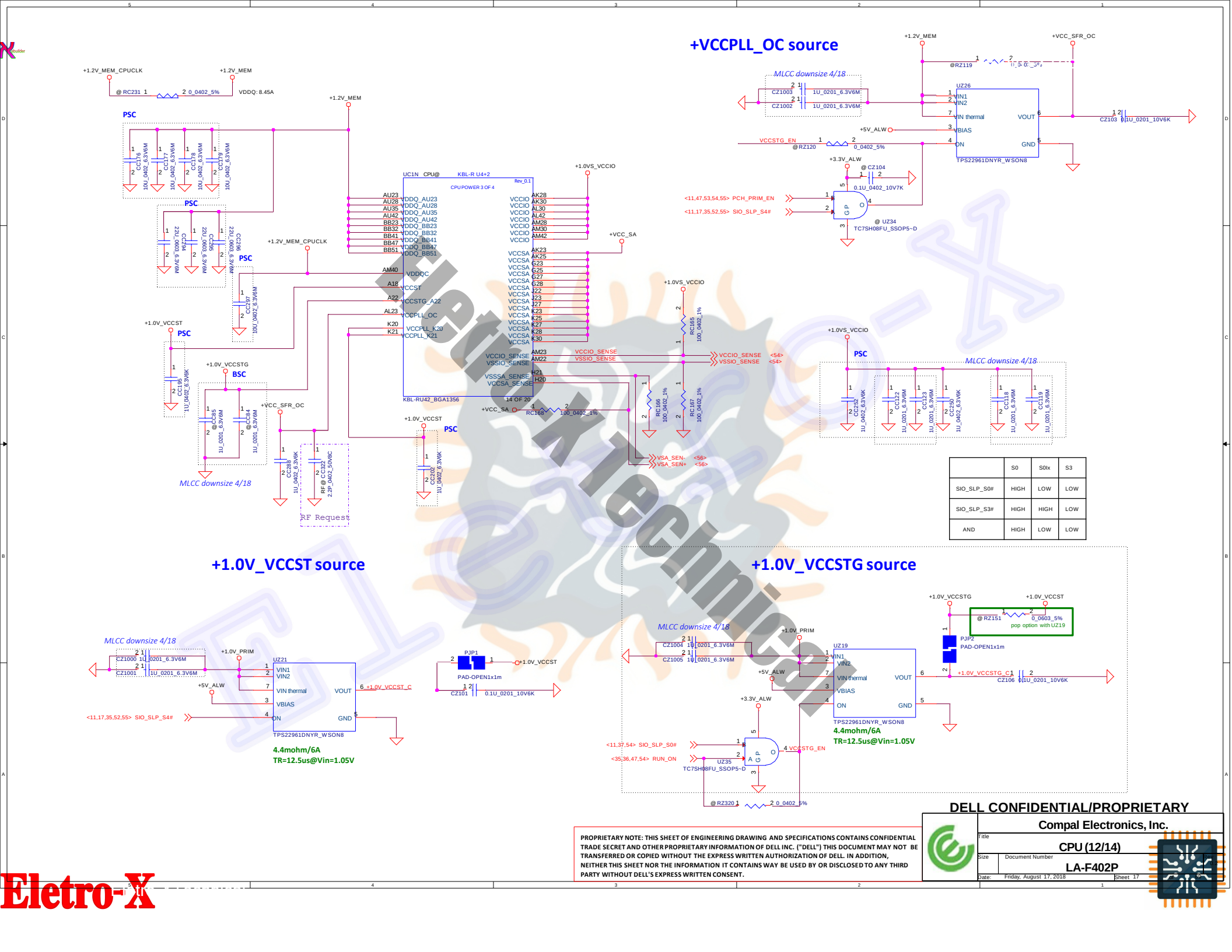
DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.

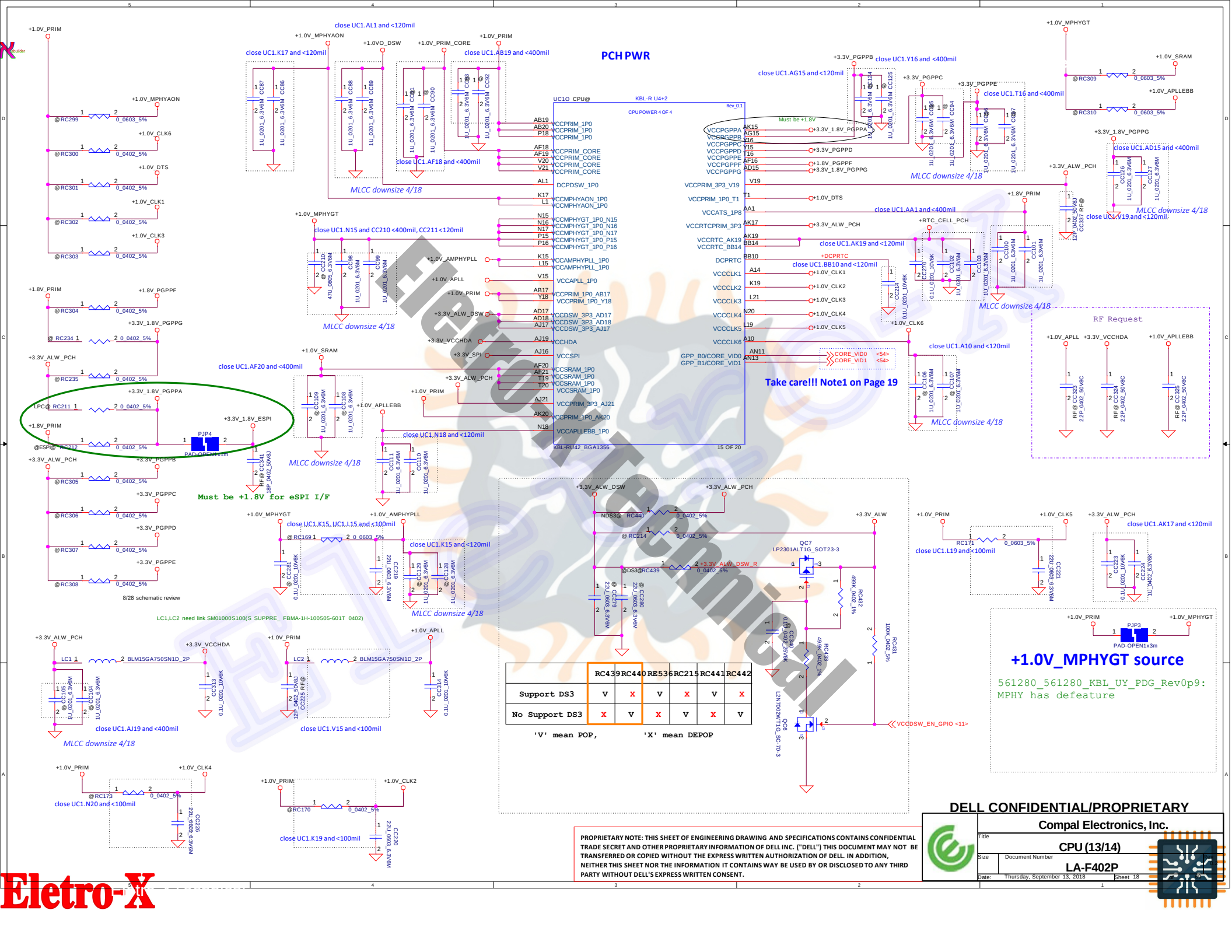
Title	CPU (11/14)	
Size	Document Number	Rev
	LA-F402P	
Date: Friday, August 17, 2018	Sheet 16	

Eletro-X



	S0	S0lx	S3
SIO_SLP_S0#	HIGH	LOW	LOW
SIO_SLP_S3#	HIGH	HIGH	LOW
AND	HIGH	LOW	LOW

Eletro-X Technical

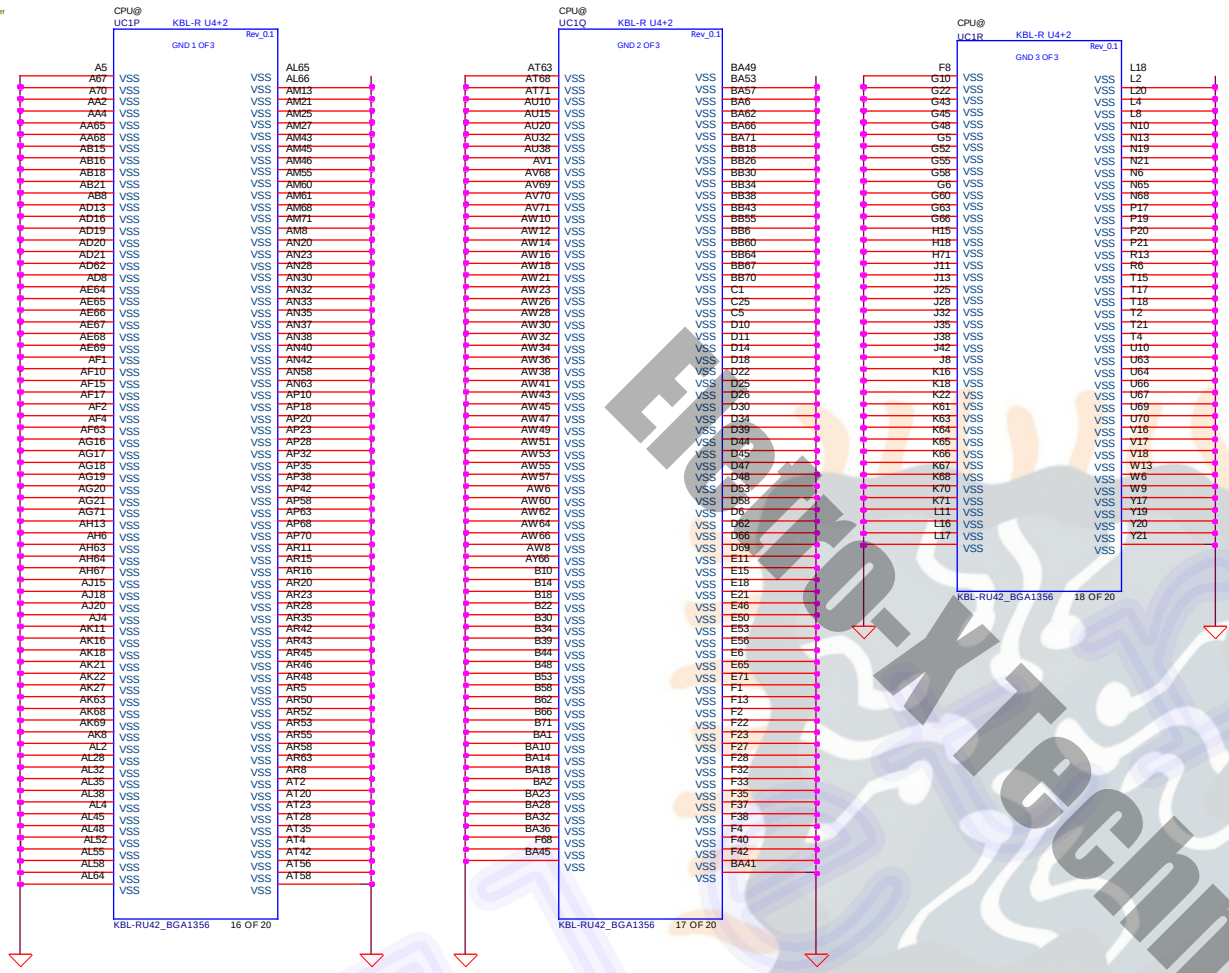


	RC439	RC440	RE536	RC215	RC441	RC442
Support DS3	V	X	V	X	V	X
No Support DS3	X	V	X	V	X	V

Eletro-X Technical

Note1: VCCPRIM_CORE Implementation with PCH CORE_VID Recommendation

R1: PR408,PR411 ; R2: PR417,PR418 ; R3,PR419,PR420 ; R4: PR423 ; R5: PR424



Eletro-X Technical

DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.

Title: CPU (14/14)

Size: | Document Number: LA-F402P | Rev:

Date: Friday, August 17, 2018 | Sheet 19

Eletro-X

For DDR4

Layout Note:
Place near JDIMM1

Layout Note:
Place near
JDIMM1.258

MLCC downsize 4/18

DIMM Select

	SA0	SA1	SA2
DIMM1	0	0	0
DIMM2	1	0	0
DIMM3	0	1	0
DIMM4	1	1	0

6/8 Change to SA00007WE00 DII

LINK DAN05-Q0406-0103 DONE

Eletro-X Technical

DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.

Title: DDR4

Size: | Document Number: LA-F402P | Rev: 0.2

Date: Friday, August 17, 2018 | Sheet: 27 of 37

For DDR4

Layout Note:
Place near JDIMM2

Layout Note:
Place near
JDIMM2.258

MLCC downsize 4/18

DIMM Select

	SA0	SA1	SA2
DIMM1	0	0	0
DIMM2	1	0	0
DIMM3	0	1	0
DIMM4	1	1	1

LINK DAN05-Q0406-0103 DONE

DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.

Title: DDR4

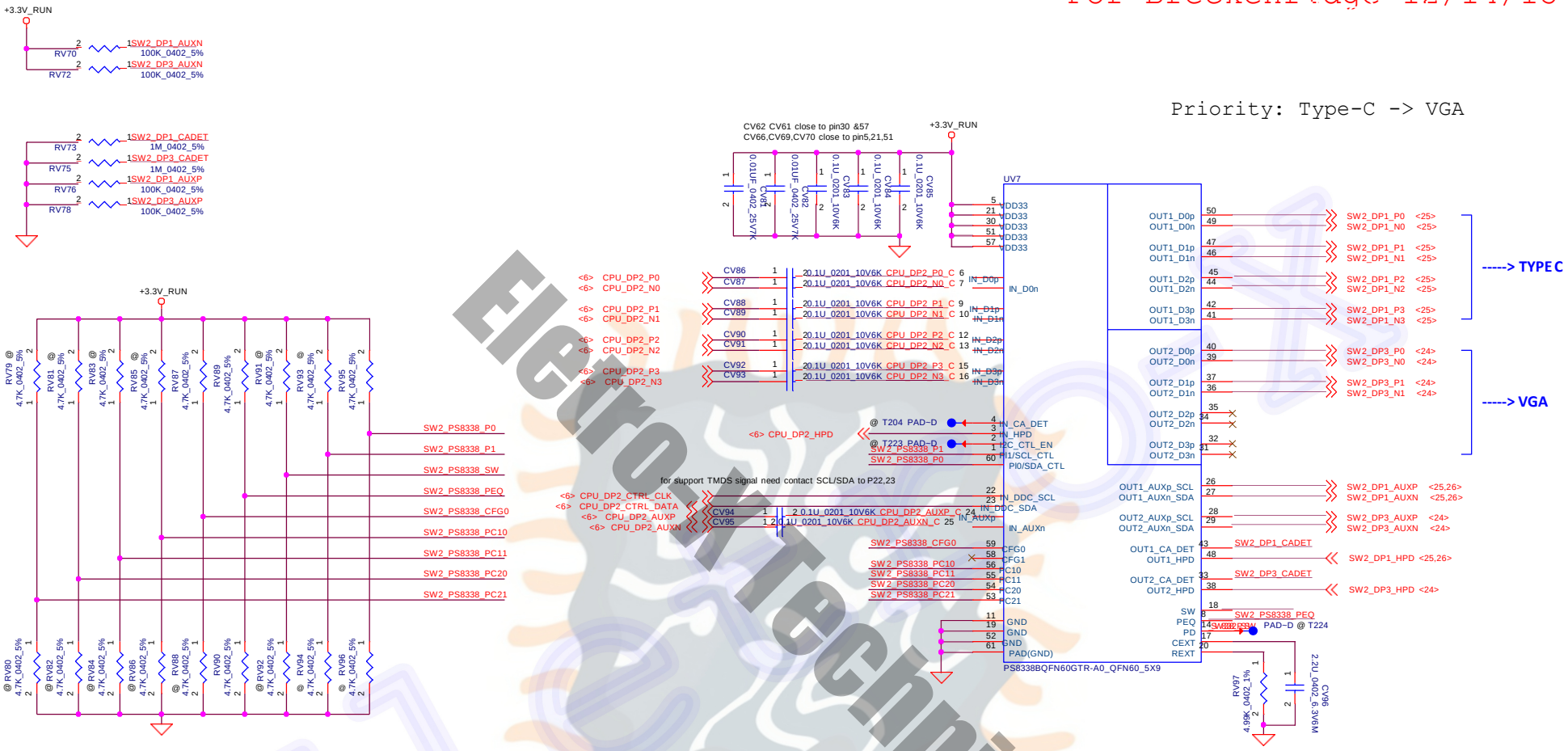
Size: | Document Number: LA-F402P | Rev: 0.2

Date: Friday, August 17, 2018 | Sheet: 25 of 44

Eletro-X Technical

For Breckenridge 12/14/15

Priority: Type-C -> VGA



Port switching control or priority configuration. Internal pull down ~150KΕ[,
3.3V I/O
For Control Switching Mode (CFG0 = L):
SW = L: Port1 is selected (default)
SW = H: Port2 is selected
For Automatic Switching Mode (CFG0 = H):
SW = L: Port1 has higher priority when both ports are plugged
SW = H: Port2 has higher priority when both ports are plugged (default)

vender suggest MUX use LLEQ PEQ=M and PI0=H !!

Programmable input equalization levels, Internal pull down at ~150Kohm,3.3V I/O
PEQ =
L: default,LEQ, compensate channel loss up to 11.5dB @HBR2
H: HEQ, compensate channel loss up to 14.5dB @HBR2
M:LLEQ, compensate channel loss up to 8.5dB @HBR2

PI0:Automatic EQ disable, Internal pull down ~150K ohm, 3.3V I/O
PI0 = L: Automatic EQ enable(default)
H: Automatic EQ disable

Eletro-X Technical

DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.

Title: DP SW2 PS8348B

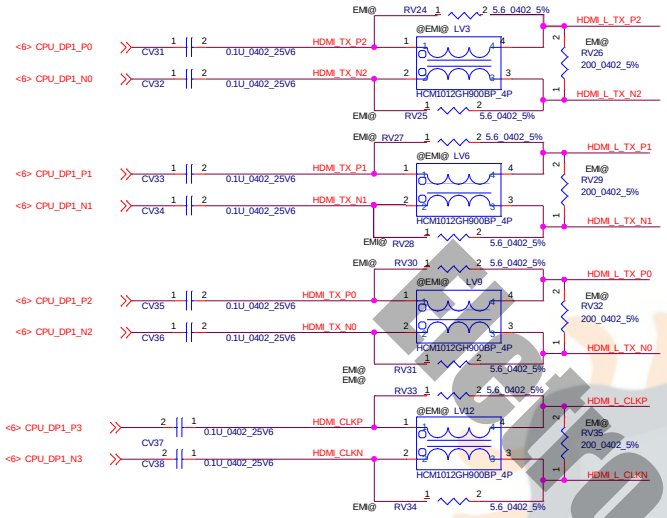
Size: Document Number: LA-F402P

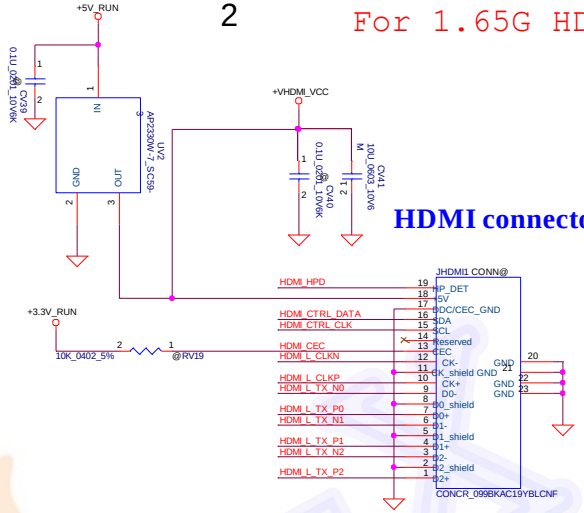
Date: Friday, August 17, 2018 Sheet 22 of

Eletro-X

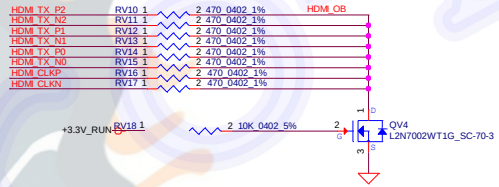
For 1.65G HDMI from CPU

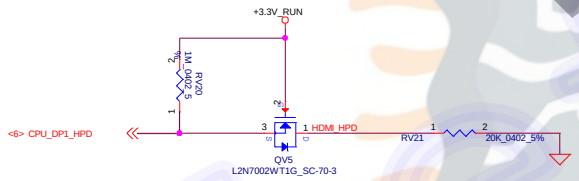
HDMI connector

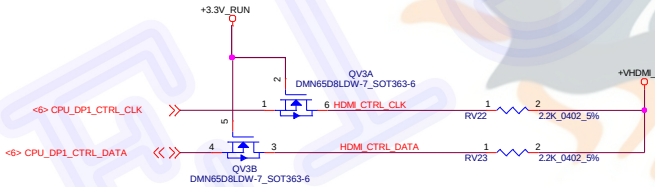




LINK 099BKAC19YBLCNF DONE







Eletro-X Technical

DELL CONFIDENTIAL/PROPRIETARY

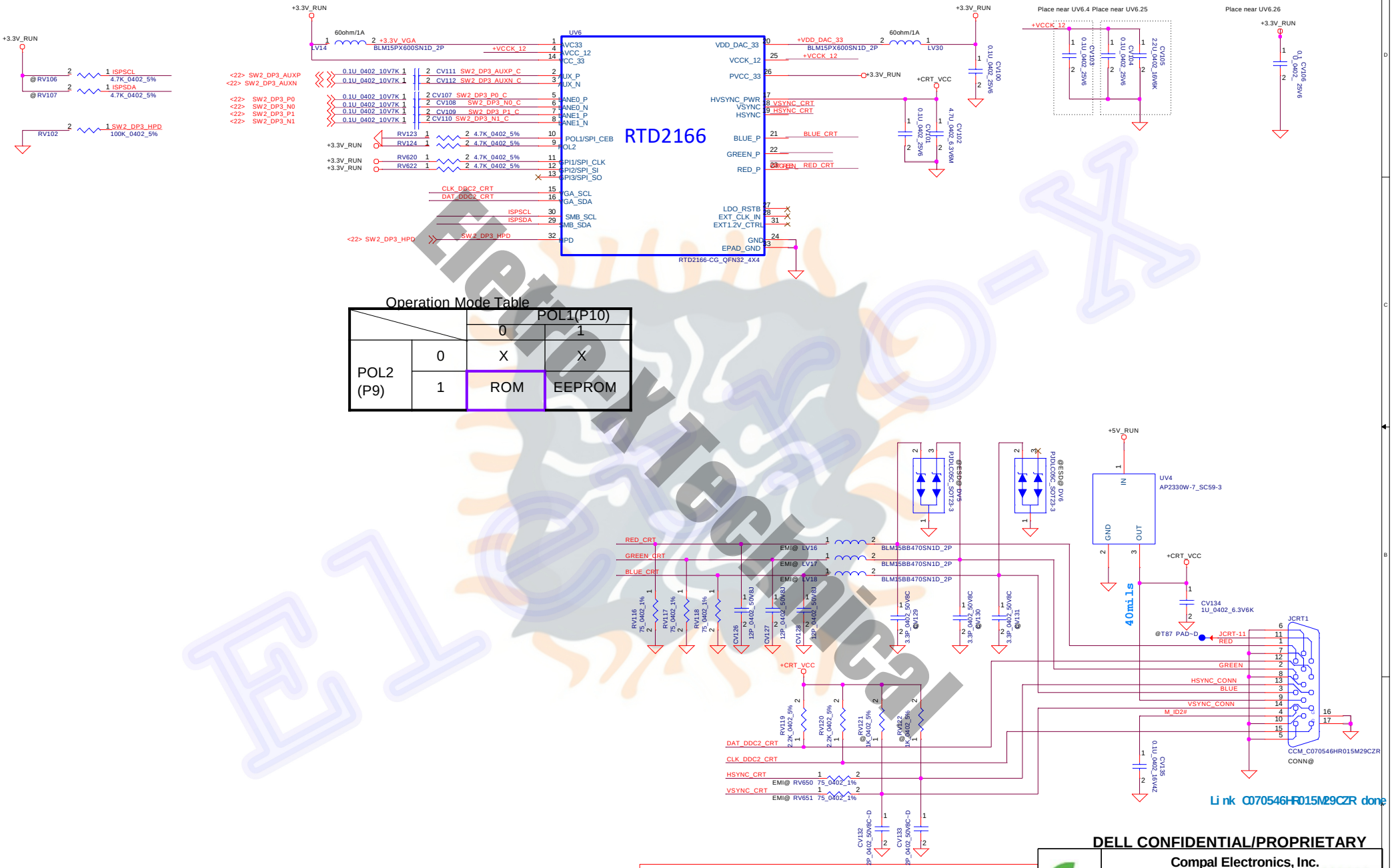
PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.

Title	HDMI CONN	
Size	Document Number	LA-F402P
Date:	Friday, August 17, 2018	Sheet 29 of 45

Eletro-X

For Breckenridge 12/14/15
For Realtek Solution



Operation Mode Table

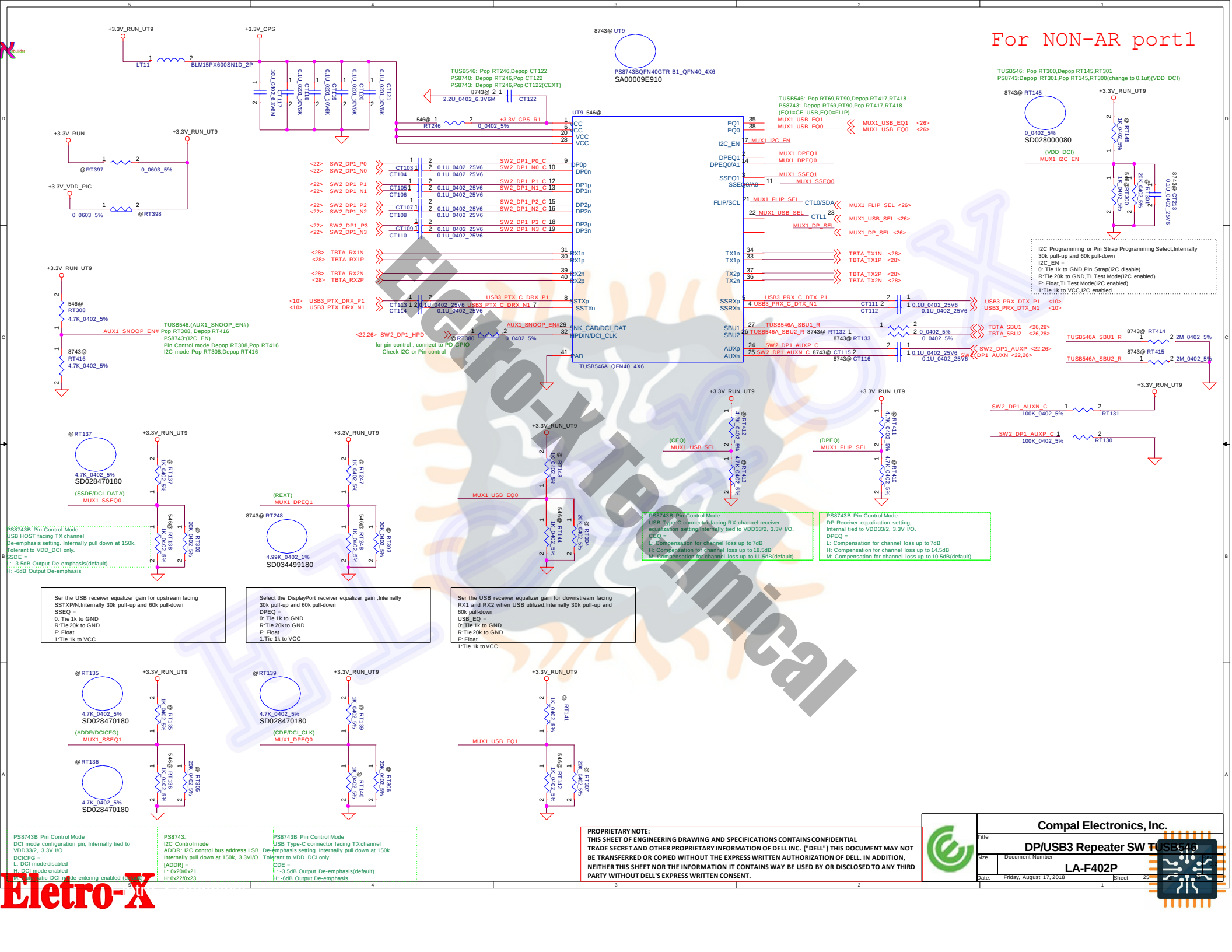
		POL1(P10)	
		0	1
POL2 (P9)	0	X	X
	1	ROM	EEPROM

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.	
Title	DP to VGA & VGA Conn
Size	Document Number: LA-F402P
Date: Friday, August 17, 2018	Sheet 24

Eletro-X


For NON-AR port1
+3.3V_RUN_UT9
+3.3V_CPS
LT11
BLM15PX600SN1D_2P
8743@ UT9
PS8743BQFN40GTR-B1_QFN40_4X6
SA00009E910
TUSB546: Pop RT246,Depop CT122
PS8740: Depop RT246,Pop CT122
PS8743: Depop RT246,Pop CT122(CEXT)
2.2U_0402_6.3V6M
CT122
UT9 546@
RT246
0_0402_5%
+3.3V_CPS_R1
TUSB546: Pop RT69,RT90,Depop RT417,RT418
PS8743: Depop RT69,RT90,Pop RT417,RT418
(EQ1=CE_USB,EQ0=FLIP)
TUSB546: Pop RT300,Depop RT145,RT301
PS8743:Depop RT301,Pop RT145,RT300(change to 0.1uf)(VDD_DCI)
8743@ RT145
SD028000080
(VDD_DCI)
MUX1_I2C_EN
+3.3V_RUN
+3.3V_VDD_PIC
@RT397
@RT398
0_0603_5%
I2C Programming or Pin Strap Programming Select,Internally 30k pull-up and 60k pull-down
I2C_EN =
0: Tie 1k to GND,Pin Strap(I2C disable)
R:Tie 20k to GND,TI Test Mode(I2C enabled)
F: Float,TI Test Mode(I2C enabled)
1:Tie 1k to VCC,I2C enabled
TUSB546:(AUX1_SNOOP_EN#)
Pop RT308, Depop RT416
PS8743:(I2C_EN)
Pin Control mode Depop RT308,Pop RT416
I2C mode Pop RT308,Depop RT416
AUX1_SNOOP_EN#
546@ RT308 4.7K_0402_5%
8743@ RT416 4.7K_0402_5%
for pin control , connect to PD GPIO
Check I2C or Pin control
TUSB546A_QFN40_4X6
MUX1_USB_EQ1
MUX1_USB_EQ0
MUX1_I2C_EN
MUX1_DPEQ1
MUX1_DPEQ0
MUX1_SSEQ1
MUX1_SSEQ0
MUX1_FLIP_SEL
MUX1_USB_SEL
MUX1_DP_SEL
TBTA_TX1N
TBTA_TX1P
TBTA_TX2P
TBTA_TX2N
TBTA_SBU1
TBTA_SBU2
SW2_DP1_AUXP
SW2_DP1_AUXN
USB3_PRX_DTX_P1
USB3_PRX_DTX_N1
USB3_PTX_DRX_P1
USB3_PTX_DRX_N1
SW2_DP1_P0
SW2_DP1_P1
SW2_DP1_P2
SW2_DP1_P3
SW2_DP1_HPD
AUX1_SNOOP_EN#
@RT137
@RT247
@RT143
@RT412
@RT411
@RT413
@RT410
(CEQ)
(DPEQ)
(SSDE/DCI_DATA)
(REXT)
(ADDR/DCICFG)
(CDE/DCI_CLK)
SD028470180
SD034499180
8743@ RT248
4.99K_0402_1%
PS8743B Pin Control Mode
USB HOST facing TX channel
De-emphasis setting. Internally pull down at 150k.
Tolerant to VDD_DCI only.
SSDE =
L: -3.5dB Output De-emphasis(default)
H: -6dB Output De-emphasis
PS8743B Pin Control Mode
USB Type-C connector facing RX channel receiver equalization setting;Internally tied to VDD33/2, 3.3V I/O.
CEQ =
L: Compensation for channel loss up to 7dB
H: Compensation for channel loss up to 18.5dB
M: Compensation for channel loss up to 11.5dB(default)
PS8743B Pin Control Mode
DP Receiver equalization setting;
Internal tied to VDD33/2, 3.3V I/O.
DPEQ =
L: Compensation for channel loss up to 7dB
H: Compensation for channel loss up to 14.5dB
M: Compensation for channel loss up to 10.5dB(default)
Ser the USB receiver equalizer gain for upstream facing SSTXP/N,Internally 30k pull-up and 60k pull-down
SSEQ =
0: Tie 1k to GND
R:Tie 20k to GND
F: Float
1:Tie 1k to VCC
Select the DisplayPort receiver equalizer gain ,Internally 30k pull-up and 60k pull-down
DPEQ =
0: Tie 1k to GND
R:Tie 20k to GND
F: Float
1:Tie 1k to VCC
Ser the USB receiver equalizer gain for downstream facing RX1 and RX2 when USB utilized,Internally 30k pull-up and 60k pull-down
USB_EQ =
0: Tie 1k to GND
R:Tie 20k to GND
F: Float
1:Tie 1k to VCC
@RT135
@RT139
@RT141
@RT136
@RT140
@RT142
@RT138
@RT248
@RT144
@RT302
@RT303
@RT304
@RT305
@RT306
@RT307
@RT131
@RT130
@RT414
@RT415
2M_0402_5%
100K_0402_5%
PS8743B Pin Control Mode
DCI mode configuration pin; Internally tied to VDD33/2, 3.3V I/O.
DCICFG =
L: DCI mode disabled
H: DCI mode enabled
M: Automatic DCI mode entering enabled (default)
PS8743:
I2C Control mode
ADDR: I2C control bus address LSB. De-emphasis setting. Internally pull down at 150k.
Internally pull down at 150k, 3.3V/0. Tolerant to VDD_DCI only.
[ADDR] =
L: 0x20/0x21
H:0x22/0x23
PS8743B Pin Control Mode
USB Type-C connector facing TX channel
CDE =
L: -3.5dB Output De-emphasis(default)
H: -6dB Output De-emphasis
PROPRIETARY NOTE:
THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL
TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT
BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION,
NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD
PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.
Compal Electronics, Inc.
Title
DP/USB3 Repeater SW TUSB546
Size
Document Number
LA-F402P
Date: Friday, August 17, 2018
Sheet 25
Elero-X Technical

For NON-AR port1

DIV = R2/(R1+R2)		Factory Device Configuration	Description
DIV_min	DIV_max		
0.00	0.08	0	UFP only 5V @0.9A Sink capability with "Ask for Max" for anything from 0.9 -3.0A TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported
0.10	0.18	1	UFP only 5V @0.9A Sink capability with "Ask for Max" for anything from 0.9 -3.0A TBT Alternate Modes not supported DisplayPort Alternate Modes -Sink, C and D pin configuration TI VID supported
0.20	0.28	2	UFP only 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported
0.30	0.38	3	UFP only 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes -Sink, C and D pin configuration TI VID supported
0.40	0.48	4	DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported Accepts data and power role swaps, but does not initiate.
0.50	0.58	5	DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes - Source, C, D, and E pin configurations. TI VID supported Accepts power role swaps but will not initiate. Accepts data role swap to UFP and can initiate.
0.60	0.68	6	DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes - Source, C, D, and E pin configurations. TI VID supported Accepts power role swaps but will not initiate. Accepts data role swap to DFP and can initiate.
0.70	1.00	7	Infinite boot retry from Flash to Host I/F cycles.

Route in pass through manner so AUX can be snooped by 546

Link TPS65982D (from SA00009W200 to SA00009W210) 08/04
running change from SA00009W210 to SA0000AK400 12/31

DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIA TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

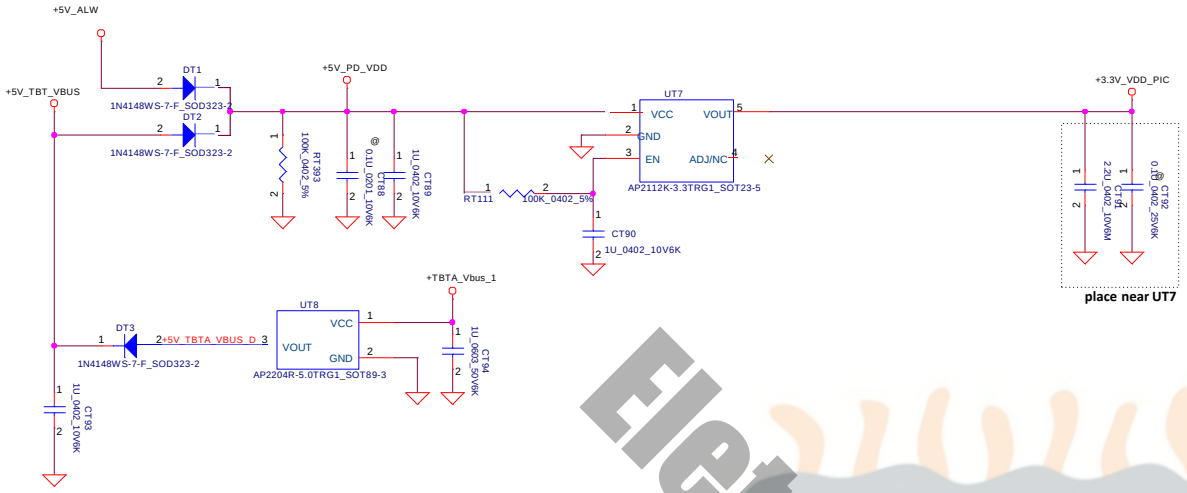
Compal Electronics, Inc.

Title: [Type C]PD Controller TI

Size: | Document Number: LA-F391P | Rev: 0.2

Date: Friday, August 17, 2018 | Sheet 2 of 57

Eletro-X
Eletrônica



Eletro-X Technical

DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.

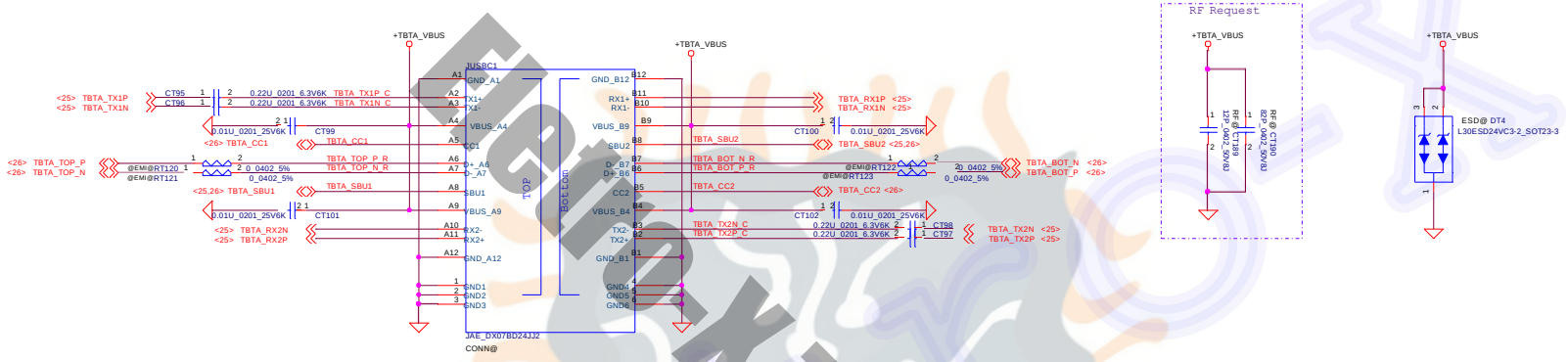
Title: [Type C]PD Power

Size | Document Number: LA-F402P

Date: Friday, August 17, 2018 | Sheet 27

Eletro-X

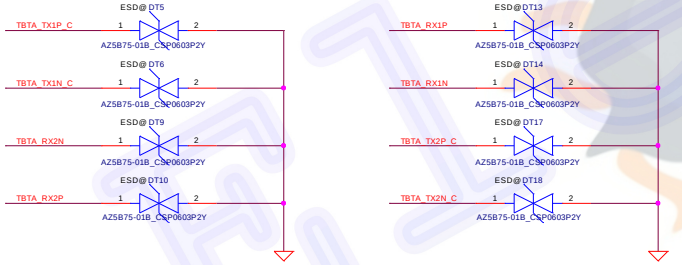
For NON AR Config

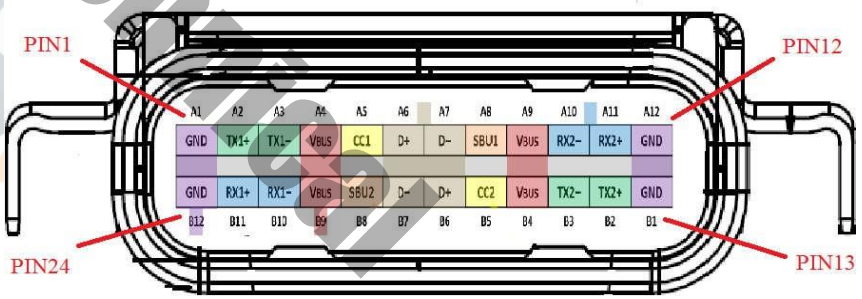


DX07BD24JJ2 LINK DONE

Premium 12/14/15 UMA:Check SBU1/SBU2 connect to PD or PS8740B

DT5, DT6, DT9, DT10, DT13, DT14, DT17,DT18,
change CPN from SC40000AT00 to SC40000DF00 06/07/2017





PROPRIETARY NOTE:
THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

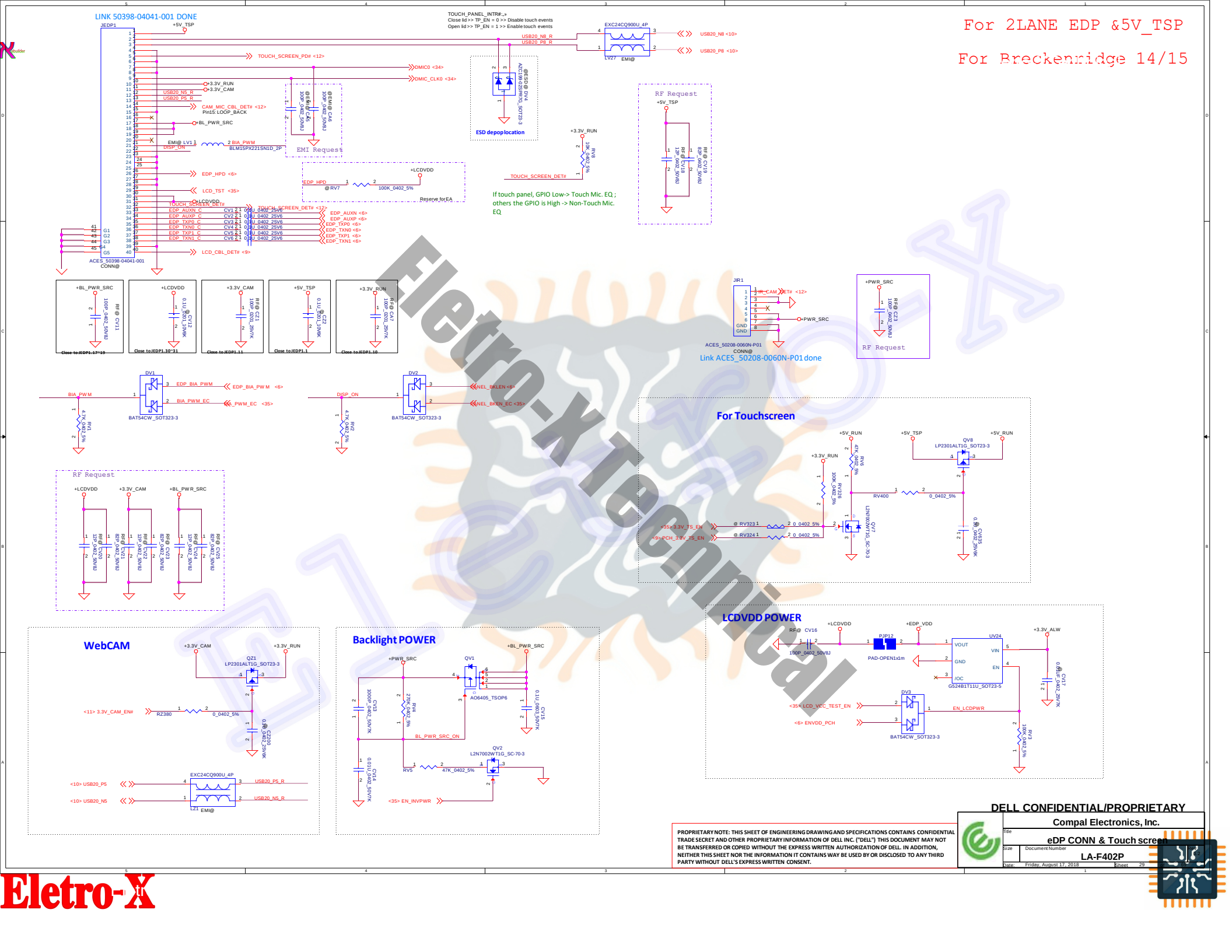
Compal Electronics, Inc.

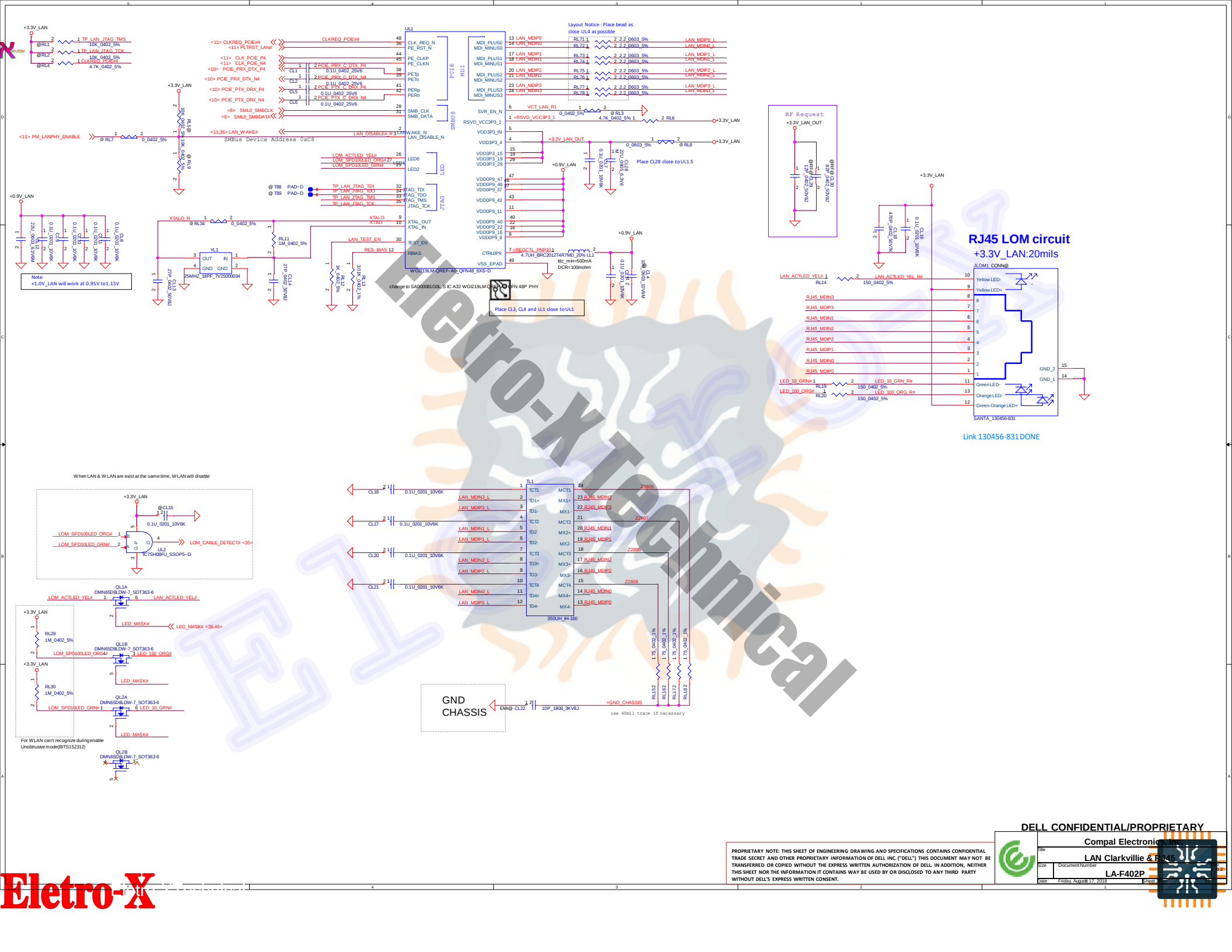
Title: USB 3.0 CONN TYPE-C

Size: Document Number: LA-F402P

Date: Friday, August 17, 2018 Sheet 28 of

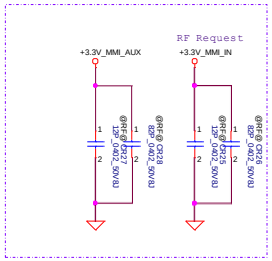
Eletro-X

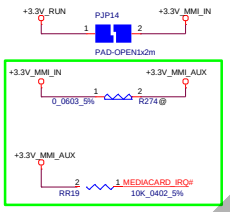

For 2LANE EDP &5V_TSP
For Breckenridge 14/15
LINK 50398-04041-001 DONE
JEDP1
+5V_TSP
TOUCH_PANEL_INTR#_»
Close lid>> TP_EN = 0 >> Disable touch events
Open lid>> TP_EN = 1 >> Enable touch events
EXC24CQ900U_4P
LV27
EMI@
USB20_N8 <10>
USB20_P8 <10>
USB20_N8_R
USB20_P8_R
TOUCH_SCREEN_PD# <12>
DMIC0 <34>
DMIC_CLK0 <34>
+3.3V_RUN
+3.3V_CAM
USB20_N5_R
USB20_P5_R
CAM_MIC_CBL_DET# <12>
Pin15:LOOP_BACK
+BL_PWR_SRC
EMI@ LV1
BLM15PX221SN1D_2P
DISP_ON
EMI Request
ESD depoplocation
EDP_HPD <6>
LCD_TST <35>
+LCDVDD
TOUCH_SCREEN_DET#
TOUCH_SCREEN_DET# <12>
EDP_AUXN_C
EDP_AUXP_C
EDP_TXP0_C
EDP_TXN0_C
EDP_TXP1_C
EDP_TXN1_C
EDP_AUXN <6>
EDP_AUXP <6>
EDP_TXP0 <6>
EDP_TXN0 <6>
EDP_TXP1 <6>
EDP_TXN1 <6>
LCD_CBL_DET# <9>
ACES_50398-04041-001
CONN@
EDP_HPD
@ RV7
100K_0402_5%
Reserve for EA
If touch panel, GPIO Low-> Touch Mic. EQ ; others the GPIO is High -> Non-Touch Mic. EQ
RF Request
+BL_PWR_SRC
+LCDVDD
+3.3V_CAM
+5V_TSP
+3.3V_RUN
Close to JEDP1.17~19
Close to JEDP1.30~31
Close to JEDP1.11
Close to JEDP1.1
Close to JEDP1.10
JIR1
IR_CAM_DET# <12>
+PWR_SRC
ACES_50208-0060N-P01
CONN@
Link ACES_50208-0060N-P01 done
DV1
BAT54CW_SOT323-3
BIA_PWM
EDP_BIA_PWM <6>
BIA_PWM_EC <35>
DV2
DISP_ON
PANEL_BKLEN <6>
PANEL_BKEN_EC <35>
For Touchscreen
QV8
LP2301ALT1G_SOT23-3
QV7
L2N7002WT1G_SC-70-3
<35> 3.3V_TS_EN
<9> PCH_3.3V_TS_EN
WebCAM
QZ1
LP2301ALT1G_SOT23-3
<11> 3.3V_CAM_EN#
RZ380
Backlight POWER
QV1
AO6405_TSOP6
QV2
L2N7002WT1G_SC-70-3
BL_PWR_SRC_ON
<35> EN_INVPWR
LCDVDD POWER
PJP12
PAD-OPEN1x1m
UV24
G524B1T11U_SOT23-5
DV3
BAT54CW_SOT323-3
<35> LCD_VCC_TEST_EN
<6> ENVDD_PCH
EN_LCDPWR
+EDP_VDD
+3.3V_ALW
Eletro-X Technical
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
eDP CONN & Touch screen
LA-F402P
Friday, August 17, 2018
29
PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.



Eletro-X Technical

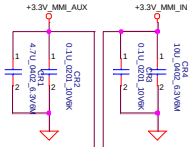
For PCIE Interface

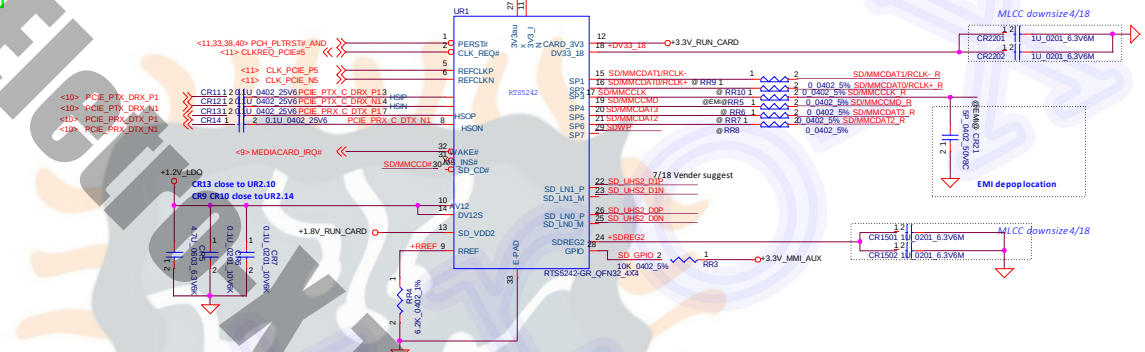




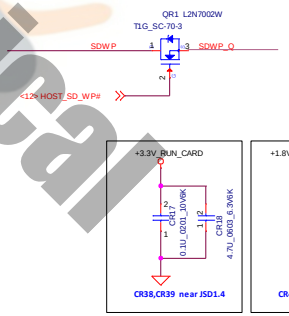
support D3 Hot(if D3 cold PIN11,PIN27 need Add MOS on/off 3V3AUX)

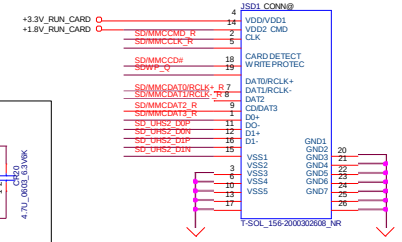
7/18 Vender suggest.





HOST_SD_WP#	SDWP_Q	SDWP	STATUS
High	High	High	Write Protect(SD LOCK)
	Low	Low	Write Enable
Low	High	High	Write Protect(SD& FW LOCK)
	Low	High	Write Protect(FW LOCK)





LINK SP070011U00 DONE

DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.

Title: Card Reader RTS5242

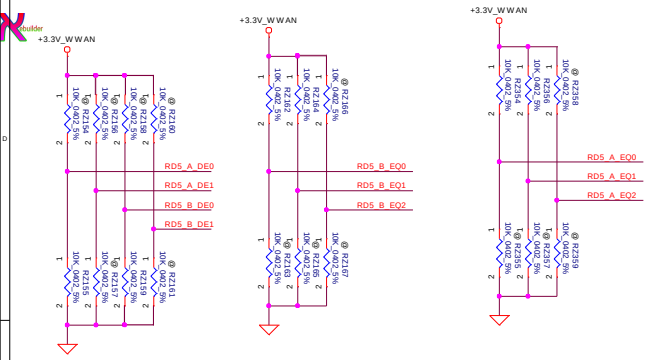
Size: | Document Number: LA-F402P | Rev: 0.2

Date: Friday, August 17, 2018 | Sheet

Eletro-X

PCIE Repeater for 3042

Only for BR15U_UMA&BR14U_UMA



	PCIE/SATA Redriver for 3042
Brekenridge12	No need
Brekenridge14U UMA	Need
Brekenridge14U DSC	No need
Brekenridge15U UMA	Need
Brekenridge15U DSC	No need
Steamboat12	No need
Steamboat14	No need
Kirkwood12&13	No need

Programmable output de-emphasis level setting for channel A .
A_DE0: internally pulled up at ~150K;
A_DE1 internally pulled down at ~150K

[A_DE1,A_DE0] ==
- LL: -2dB
- HL: -7.5dB
- LH: -3.5dB (default)
- HH: -6dB

Programmable output de-emphasis level setting for channel B.
B_DE0: internally pulled up at ~150K;
B_DE1 internally pulled down at ~150K

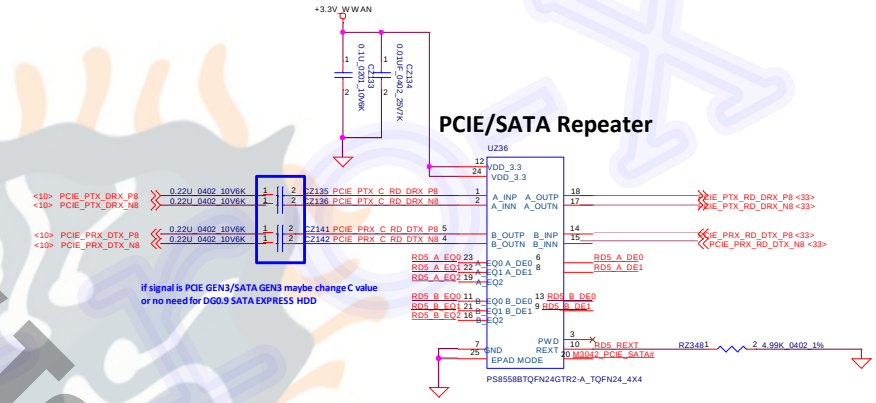
[B_DE1,B_DE0] ==
- LL: -2dB
- HL: -7.5dB
- LH: -3.5dB (default)
- HH: -6dB

Equalizer control and program for channel A.
A_EQ0, A_EQ1 and A_EQ2: internally pulled down at ~150K

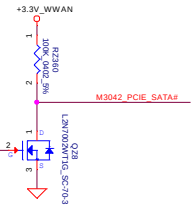
[A_EQ2,A_EQ1,A_EQ0] ==
- LLL: For channel loss up to 17dB (default)
- LHL: For channel loss up to 14dB
- HLL: For channel loss up to 19dB
- HHL: For channel loss up to 21dB
- LLH: For channel loss up to 18dB
- LHH: For channel loss up to 10dB
- HLH: For channel loss up to 16dB
- HHH: For channel loss up to 20dB

Equalizer control and program for channel B.
B_EQ0, B_EQ1 and B_EQ2: internally pulled down at ~150K

[B_EQ2,B_EQ1,B_EQ0] ==
- LLL: For channel loss up to 17dB (default)
- LHL: For channel loss up to 14dB
- HLL: For channel loss up to 19dB
- HHL: For channel loss up to 21dB
- LLH: For channel loss up to 18dB
- LHH: For channel loss up to 10dB
- HLH: For channel loss up to 16dB
- HHH: For channel loss up to 20dB



M3042_PCIE_SATA#	DEVICE interface
0	SATA
1	PCIE



SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTI TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIR PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: PCIE REPEATER for M.2 3042

Size: | Document Number: LA-F402P

Date: Friday, August 17, 2018 | Sheet 32 of

Eletro-X Technical

for no AR,Brekenridge 12/14/15 UMA/Steamboat

NGFF slot B Key B

support SATA/PCIE

9/24:Reserve for embedded location ,refer Intel PDG 0.9

NGFF slot A Key A

WLAN

9/24:Reserve for embedded location ,refer Intel PDG 0.9

SIM Card PushPush

T-SOL_5-991503004000-6 LINK DONE

STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type	M3042_PCIE#_SATA
0	GND	GND	GND	GND	SSD-SATA	High
1	GND	HIGH	GND	GND	SSD-PCIE(2 lane)	Low
8	HIGH	GND	GND	GND	WWAN	Low
14	HIGH	GND	HIGH	HIGH	HCA-PCIE(1 lane)	Low
15	HIGH	HIGH	HIGH	HIGH	NA	Low

Power Rating TBD

PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V				

Eletro-X Technical

DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.

Title: NGFF Card

Size: | Document Number: LA-F402P | Rev: 0.2

Date: Friday, August 17, 2018 | Sheet: 27 of 31

1W x 1ch, 4ohm (Transducer spec is 8Ohm/0.5W att per unit, there are two transducer units in one speaker box.)

Internal Speakers Header

40 mils trace keep 20 mil spacing

CONN@ JSPK1 ACES_50278-00401-001

Link 50278-00401-001 DONE

Close to UA1

Close to UA1 pin6

place close to UA1 pin3

Place closely to Pin 14.

Add for solve pop noise and detect issue

place at AGND and DGND plane

CLASS-D POWER DOWN CONTROL CIRCUIT

HDA_Link is 3.3V,no need level shift circuit

RB751S40_SOD523-2

RE313@one control line if DVDD is 3.3V
DE2@two control lines1

Power sequence +5V_RUN_AUDIO(501us) > +3.3V_RUN_AUDIO(1204 us) > +1.5V_RUN

Reserve for support D3 cold

2.5A

500mA

EM5209VF_SON14_2X3

Place CA29 close to Codec

SLEEVE/RING2 please keep 40 mils trace width

AUD_HP_OUT_L/ AUD_HP_OUT_Rplease keep 15 mils trace width

ALC3246-CG_MQFN48_6X8

HP-Out-Right

HP-Out-Left

Nokia-MIC

iPhone-MIC

Global Headset

Universal Jack

Normal

Open

Only BR15U UMA use LA2 LA3,because 8L

Link 2SJ3095-136111F DONE

Elektor Technical

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	<Deciphered_Date>

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

DELL CONFIDENTIAL/PROPRIETARY

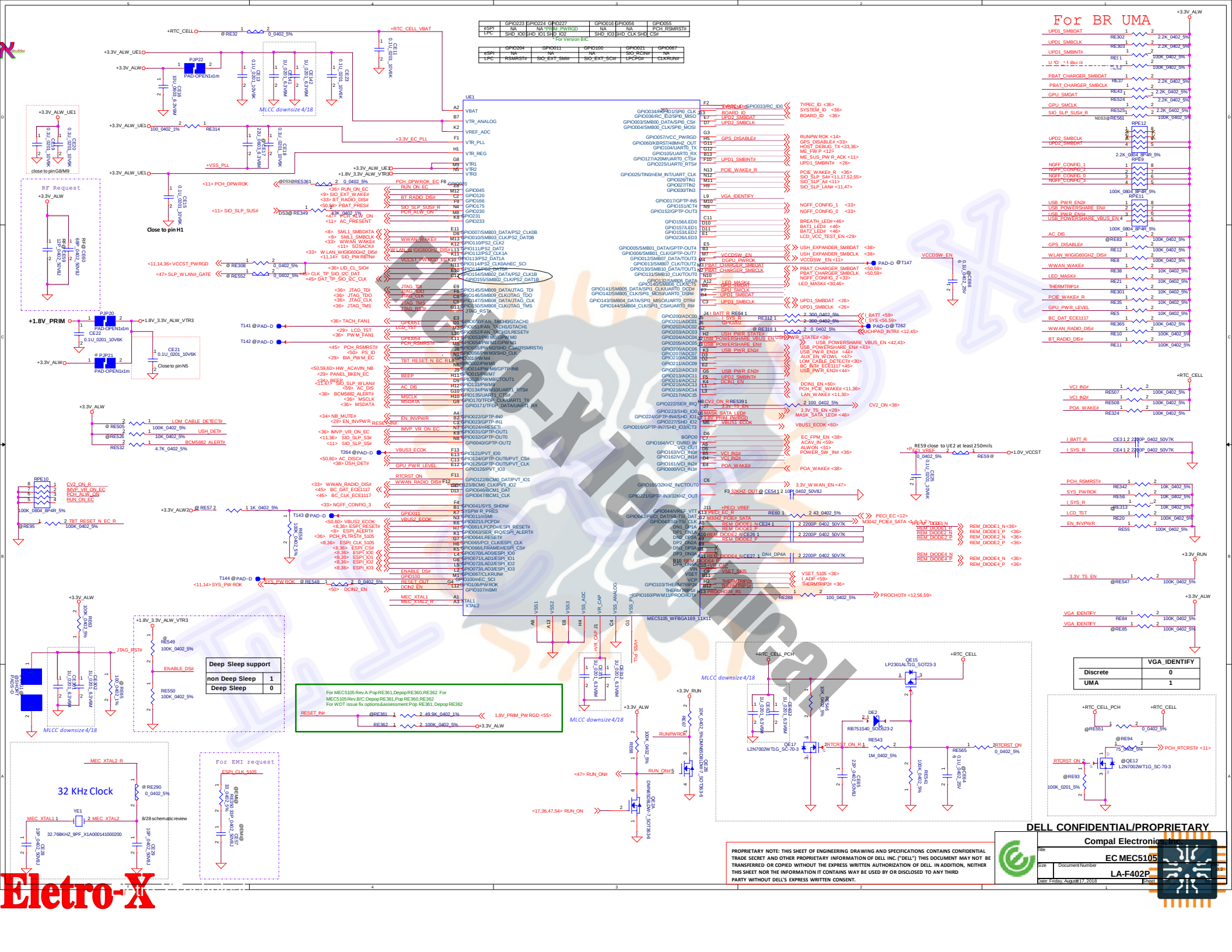
Compal Electronics, Inc.

Codec ALC3246

LA-F402P

Friday, August 17, 2018

Eletro-X


For BR UMA
UE1
MEC5105_WFBGA169_11X11
RF Request
32 KHz Clock
For EMI request
Deep Sleep support
non Deep Sleep 1
Deep Sleep 0
Discrete 0
UMA 1
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
EC MEC5105
LA-F402P
PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.
Eletro-X Technical

For BR UMA

6/8 Change to SA00007WE00 DII

PAGE	ESPI	LPC
8	RC25_10K	RC8_15ohm RC13/RC27_8.2K
18	RC212_0ohm 0603	RC211_0ohm 0603
31		RE337,RE338 RE339,RE340, RE341 0_ohm
32	RE2 / RE3 0_ohm	

JXT_FP241AH-010GAAM LINK DONE

LPC 80Port Debug	LPC	ESPI
1	+3.3V_RUN	+3.3V_RUN
2	+3.3V_RUN	+3.3V_RUN
3	LPC_LAD0	ESPI_IO0
4	LPC_LAD1	ESPI_IO1
5	LPC_LAD2	ESPI_IO2
6	LPC_LAD3	ESPI_IO3
7	LPC_FRAME#	ESPI_CS#
8	PCH_PLTRST#	NA
9	GND	GND
10	LPC_CLOCK	ESPI_CLK

6/8 Change to SA00007WE00 DII

For WHEA BSOD issue respin,
board ID change to A01(RE79=240K) 8/17

RE343	CE62	REV
* 240K	4700p	Single Port ACE w/oAR
130K	4700p	Single Port ACE w/AR
62K	4700p	Dual Port ACE w/oAR
33K	4700p	Dual Port ACE w/AR
8.2K	4700p	Dual Port ACE (w/AR +w/oAR)
4.3K	4700p	.
2K	4700p	
1K	4700p	

PD_ACE_DET# rise time is measured from 5%~68%.

RE79	CE40	REV
* 240K	4700p	A02
130K	4700p	
62K	4700p	
33K	4700p	
8.2K	4700p	
4.3K	4700p	
2K	4700p	
1K	4700p	

BOARD_ID rise time is measured from 5%~68%.

RE300	CE47	PANEL SIZE
240K	4700p	11"
130K	4700p	12"
62K	4700p	13"
* 33K	4700p	14"
8.2K	4700p	15"
4.3K	4700p	17"
2K	4700p	15P
1K	4700p	

SYSTEM_ID rise time is measured from 5%~68%.

Rest=1.69K ,Tp=97

Link 50271-0040N-001 DONE

JXT_FP241AH-010GAAM LINK DONE

Thermal diode mapping

5085 Channel	Location
DP1/DN1	CPU (QE3)
DP2/DN2	WiGig (QE5)
DN2a/DP2a	DDR (QE7)
DP3/DN3	NA
DP4/DN4	CPU VR (QE6)

Place under CPU
Place CE35 close to the QE3 as possible

DP2/DN2 for WiGig on QE5, place QE5 close to WiGig and CE37 close to QE5

DP4/DN4 for Skin on QE6, place QE6 close to Vcore VR choke.

DN2a/DP2a for DDR on QE7, place QE7 close to DDR and CE46 close to QE7

DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

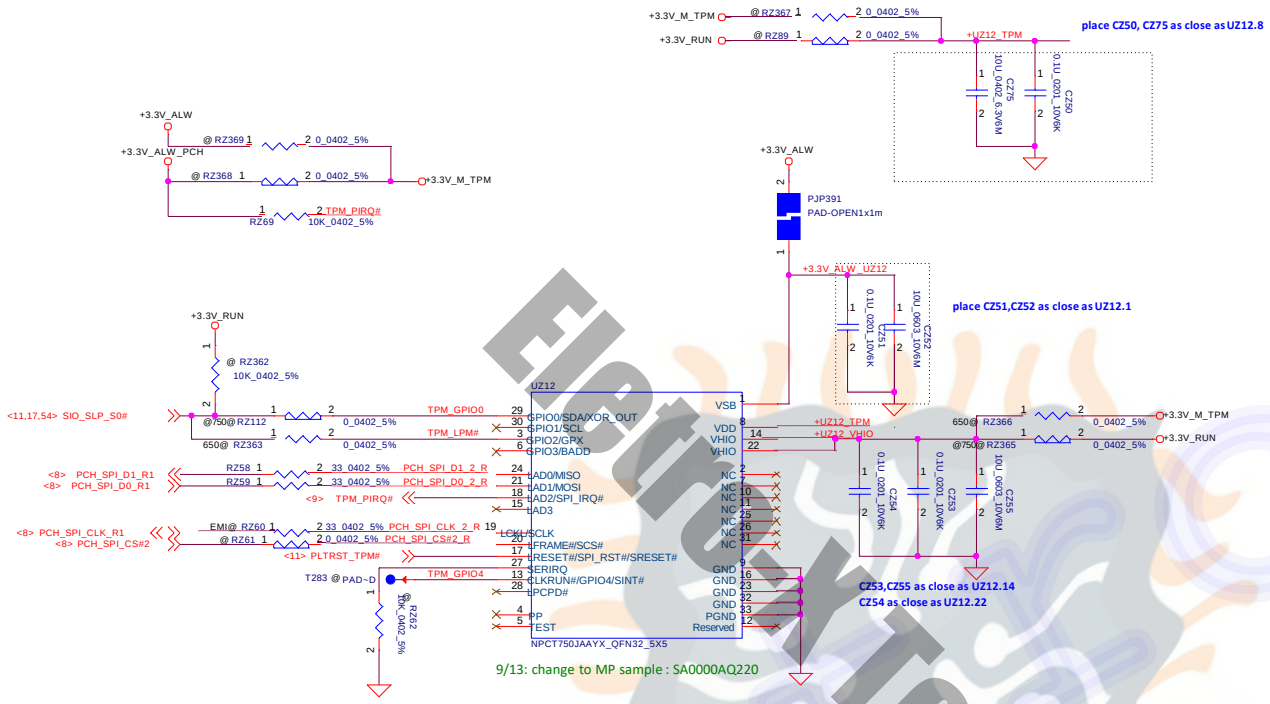
Compal Electronics, Inc.

MEC5105 Support

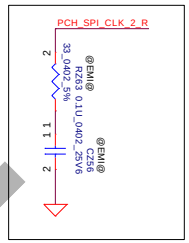
LA-F402P

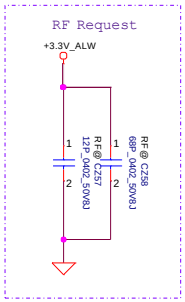
Eletro-X Technical

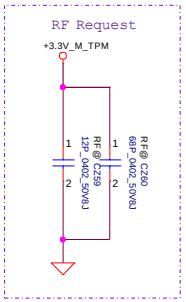
For NUVOTON TPM



	Pop	Depop	Comment
NPCT65x	RZ89, RZ366, RZ62, RZ363	RZ365, RZ367, RZ112	VDD - V_RUN Power VHIO - V_SPI Power
NPCT75x	RZ89, RZ365, RZ112	RZ367, RZ366, RZ62, RZ363	Option1 (recommended) VDD and VHIO - V_RUN power
NPCT75x	RZ367, RZ366	RZ89, RZ365, RZ62	Option2 (for Z1 sample (early sample)) VDD and VHIO - V_SPI power







Elektro-Technical

DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.

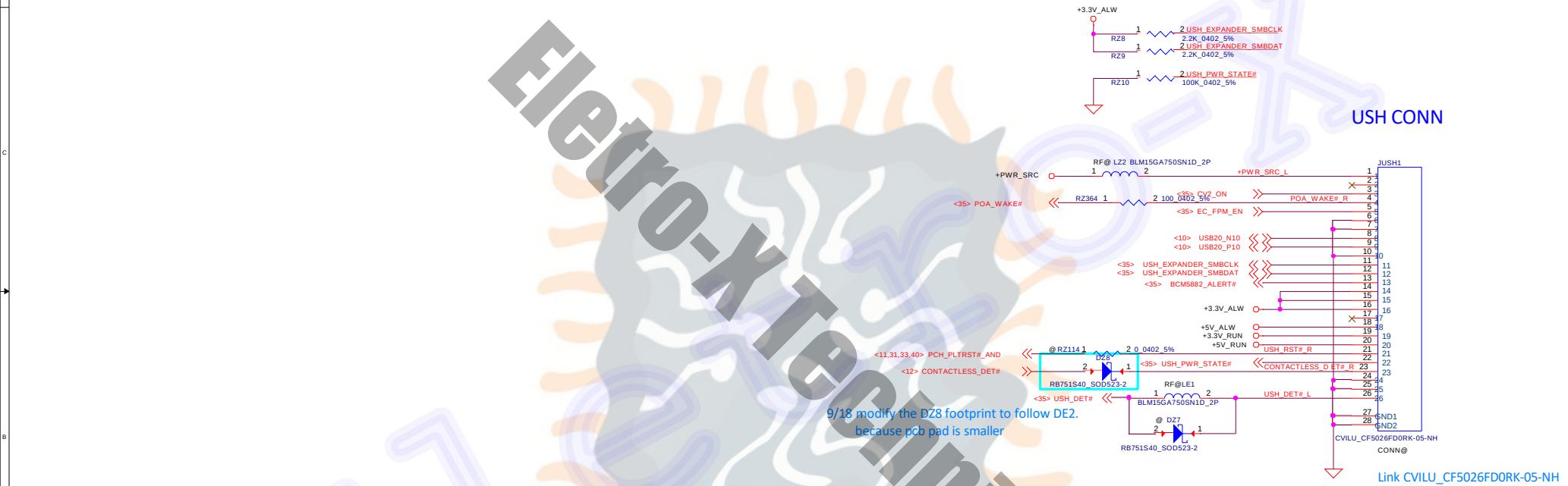
Title: USH & TPM

Size: | Document Number: LA-F402P | Rev:

Date: Friday, August 17, 2018 | Sheet 37

Eletro-X

For ATMEL TPM



Eletro-X Technical

DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.

Title	USH & TPM	
Size	Document Number	Rev
	LA-F402P	
Date: Friday, August 17, 2018	Sheet 38	

Eletro-X

For Parade 2 Lane solution

	PCIE/SATA Redriver for 2280
Brekenridge12	Need
Brekenridge14U UMA	Need
Brekenridge14U DSC	Need
Brekenridge15U UMA	Need
Brekenridge15U DSC	Need
Steamboat12	No need
Steamboat14	Need
Kirkwood12&13	Check

Programmable output de-emphasis level setting for channel A .
A_DE0: internally pulled up at ~150K;
A_DE1 internally pulled down at ~150K

[A_DE1,A_DE0] ==
LL: -2dB
HL: -7.5dB
LH: -3.5dB (default)
HH: -6dB

Programmable output de-emphasis level setting for channel B.
B_DE0: internally pulled up at ~150K;
B_DE1 internally pulled down at ~150K

[B_DE1,B_DE0] ==
LL: -2dB
HL: -7.5dB
LH: -3.5dB (default)
HH: -6dB

Equalizer control and program for channel A.
A_EQ0, A_EQ1 and A_EQ2: internally pulled down at ~150K

[A_EQ2,A_EQ1,A_EQ0] ==
LLL: For channel loss up to 17dB (default)
LHL: For channel loss up to 14dB
HLL: For channel loss up to 19dB
HHL: For channel loss up to 21dB
LLH: For channel loss up to 18dB
LHH: For channel loss up to 10dB
HLH: For channel loss up to 16dB
HHH: For channel loss up to 20dB

Equalizer control and program for channel B.
B_EQ0, B_EQ1 and B_EQ2: internally pulled down at ~150K

[B_EQ2,B_EQ1,B_EQ0] ==
LLL: For channel loss up to 17dB (default)
LHL: For channel loss up to 14dB
HLL: For channel loss up to 19dB
HHL: For channel loss up to 21dB
LLH: For channel loss up to 18dB
LHH: For channel loss up to 10dB
HLH: For channel loss up to 16dB
HHH: For channel loss up to 20dB

PCIE/SATA Repeater

PWD	Funtion
0	Normal mode(default)
1	power down mode

M2280_PCIE_SATA#	DEVICE interface
0	SATA
1	PCIE

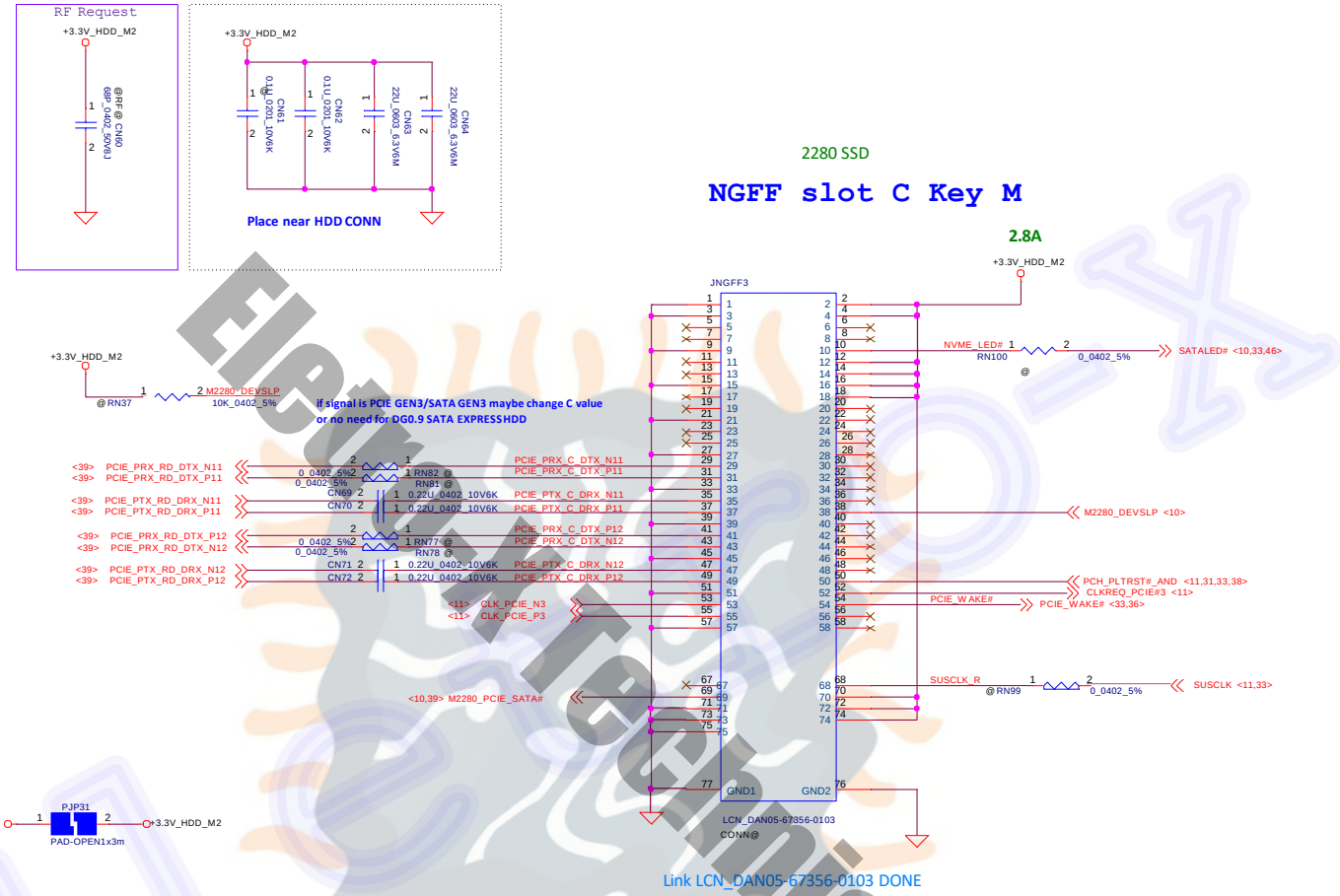
SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTI TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIR PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
Title: SATA/PCIE REPEATER for M.2 2280
Size: LA-F402P
Date: Friday, August 17, 2018
Sheet 39 of

Eletro-X Technical



PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

DELL CONFIDENTIAL/PROPRIETARY

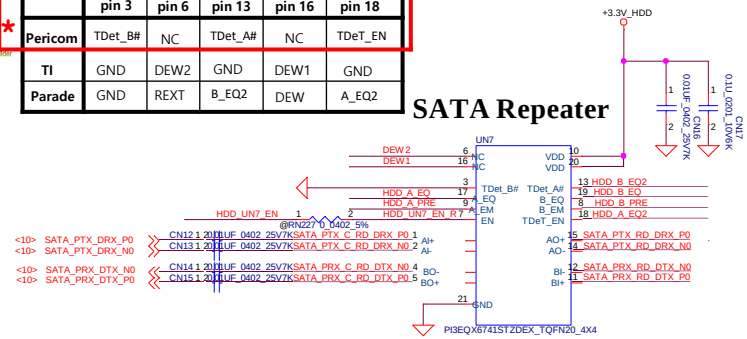
Compal Electronics, Inc.

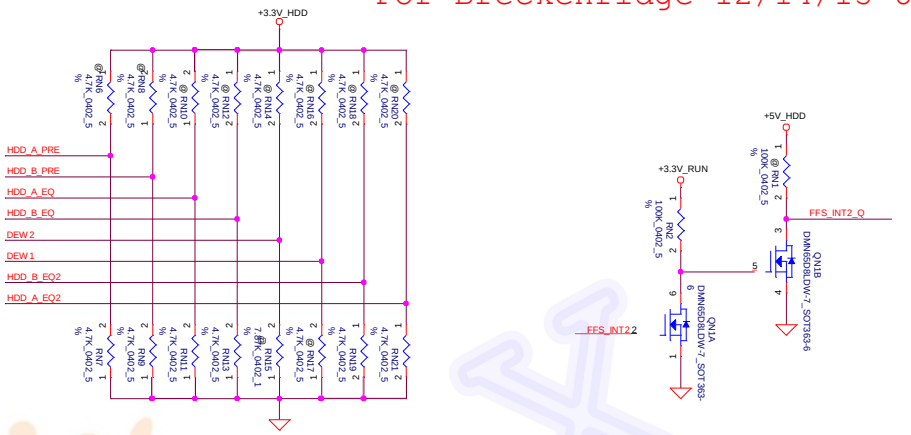
Title	M2 2280 Socket	
Size	Document Number	LA-F402P
Date: Friday, August 17, 2018	Sheet 40	

ElectroTechnical
Eletro-X

	pin 3	pin 6	pin 13	pin 16	pin 18
Pericom	TDet_B#	NC	TDet_A#	NC	TDeT_EN
TI	GND	DEW2	GND	DEW1	GND
Parade	GND	REXT	B_EQ2	DEW	A_EQ2

SATA Repeater



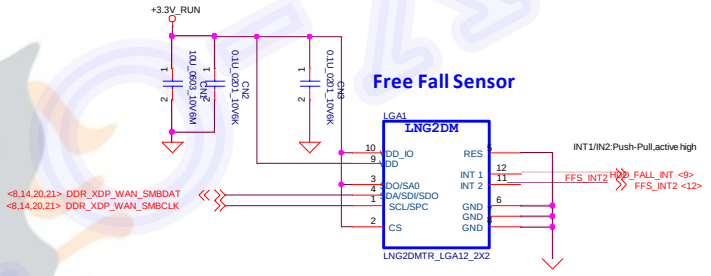


	HDD_A_EQ PIN17	HDD_B_EQ PIN19	HDD_A_EQ2 PIN18	HDD_B_EQ2 PIN13	DEW1 PIN16	DEW2 PIN6	HDD_A_PRE PIN9	HDD_B_PRE PIN8
* Pericom PI3EQX6741ST	PD (RN11)	PD (RN13)	PD (RN21)	PD (R N 19)	NC	NC	PD (R N 7)	PD (R N 9)
TI SN75LVCP601	PD (RN11)	NC	PD (RN21)	PD (R N 19)	NC (IPU)	NC (IPU)	PH (RN6)	PH (RN8)
Parade PS8527C	PD (RN11)	PD (RN13)	PD (RN21)	PD (R N 19)	NC (1/2 VDD)	PD (R N 15)	NC (1/2 VDD)	NC (1/2 VDD)

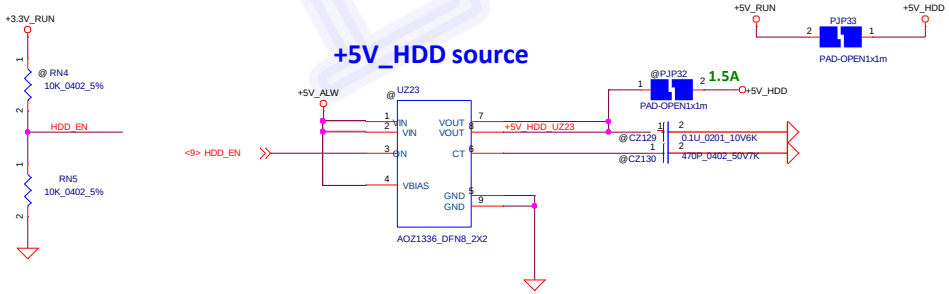
			A_EQ	B_EQ		A_EM	B_EM
* Main	Pericom	0	3dB	3dB	0	0dB	0dB
		NC	6dB	6dB	NC		
		1	9dB	9dB	1	1.5dB	1.5dB
2nd	TI	0	7dB	7dB	0	0dB	0dB
		NC	0dB	0dB	NC	-4dB	-4dB
		1	14dB	14dB	1	-2dB	-2dB
3rd	Parade	EQ2 EQ1 (M=VDD/2)	A_EQ	B_EQ		A_EM	B_EM
		0 0	2.4dB	2.4dB			
		0 M	7.4dB	7.4dB			
		0 1	14.4dB	14.4dB	0	0dB	0dB
		M M	12.2dB	12.2dB	M	-3.5dB	-3.5dB
		M 0	9.4dB	9.4dB	1	-1.5dB	-1.5dB
		M 1	13.3dB	13.3dB			
		1 M	6.2dB	6.2dB			
		1 0	11.2dB	11.2dB			
		1 1	5dB	5dB			

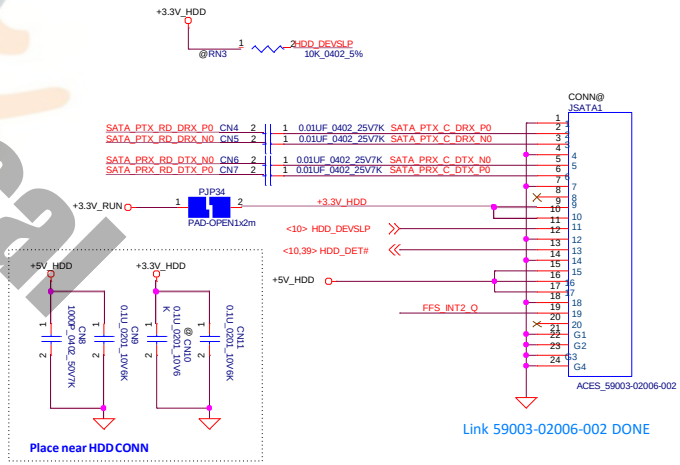
* red color is current setting

Free Fall Sensor



+5V_HDD source





PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

DELL CONFIDENTIAL/PROPRIETARY

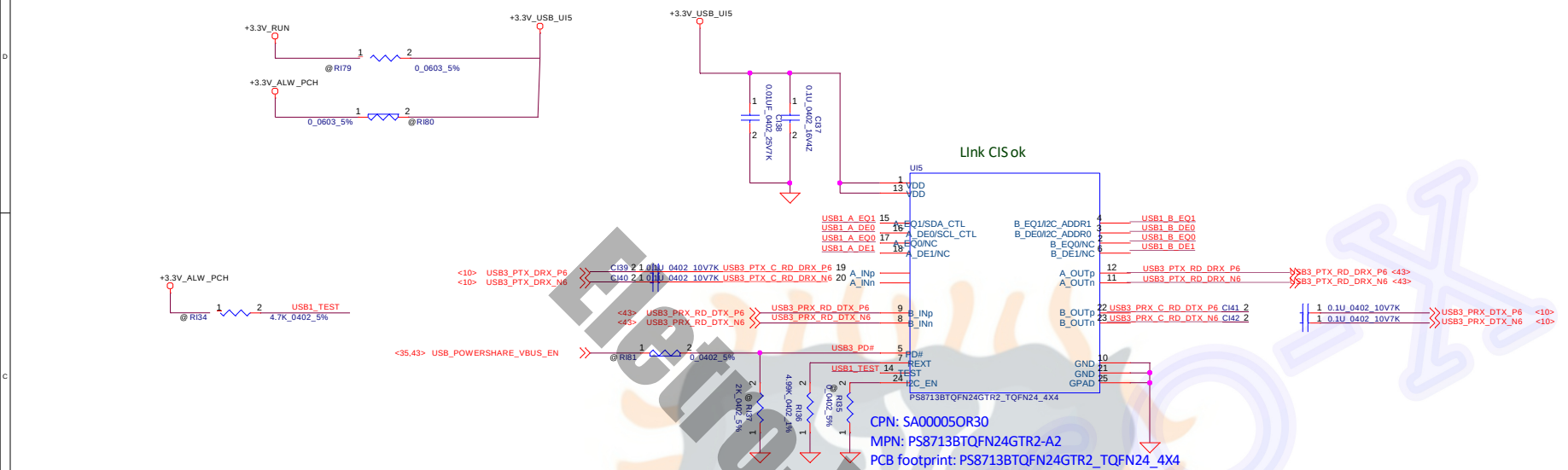
Compal Electronics, Inc.

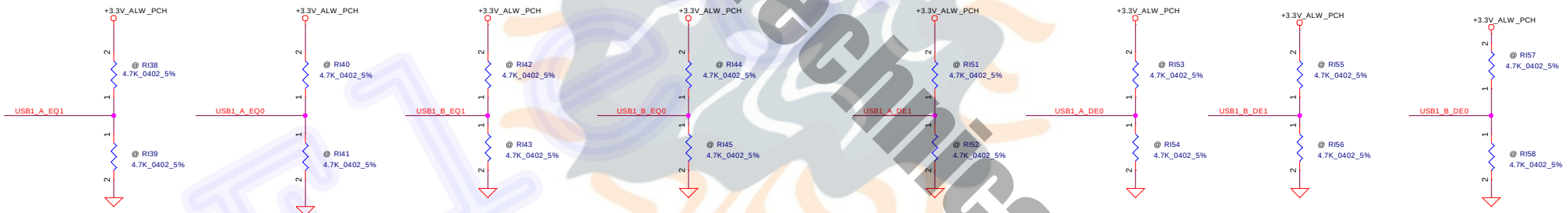
Title: SATA Repeater&HDD CONN

Size: Document Number: LA-F402P

Date: Friday, August 17, 2018 Sheet 41

Eletro-X Technical





Parade_PS8713B

A_EQ1	A_EQ0	B_EQ1	B_EQ0	Recommended EQ
0	0	0	0	loss up to 9.5dB
1	1	0	1	loss up to 13dB
2	0	1	0	loss up to 4.5dB
1	1	1	1	loss up to 7.5dB

Both A_EQ&B_EQ have internal pull-down 150k

A_DE1	A_DE0	B_DE1	B_DE0	Recommended DE
0	0	0	0	3.5dB de-emphasis
0	1	0	1	No de-emphasis
1	0	1	0	2.7dB de-emphasis
1	1	1	1	5dB de-emphasis

Both A_DE&B_DE have internal pull-down 150k

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

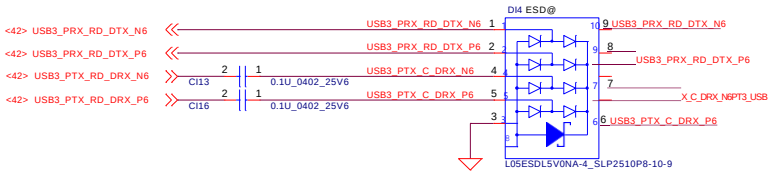
DELL CONFIDENTIAL/PROPRIETARY

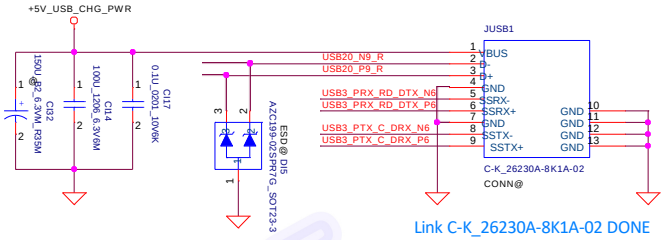
Compal Electronics, Inc.

Title	USB3.0 Repeater	
Size	Document Number	Rev
	LA-F402P	
Date: Friday, August 17, 2018	Sheet 42	

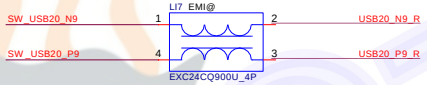
Eletro-X Technical

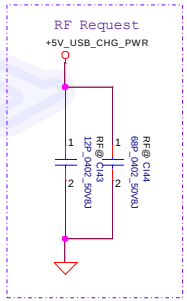
For w/ Repeater

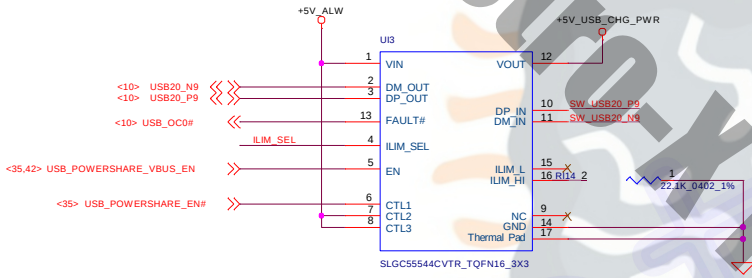




Link C-K_26230A-8K1A-02 DONE

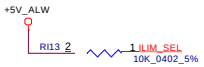


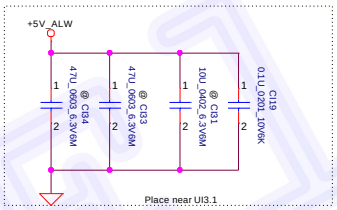




Link Seligro SA000097E10 Done

MAIN:SLGC55544CVTR





Eletro-X Technical

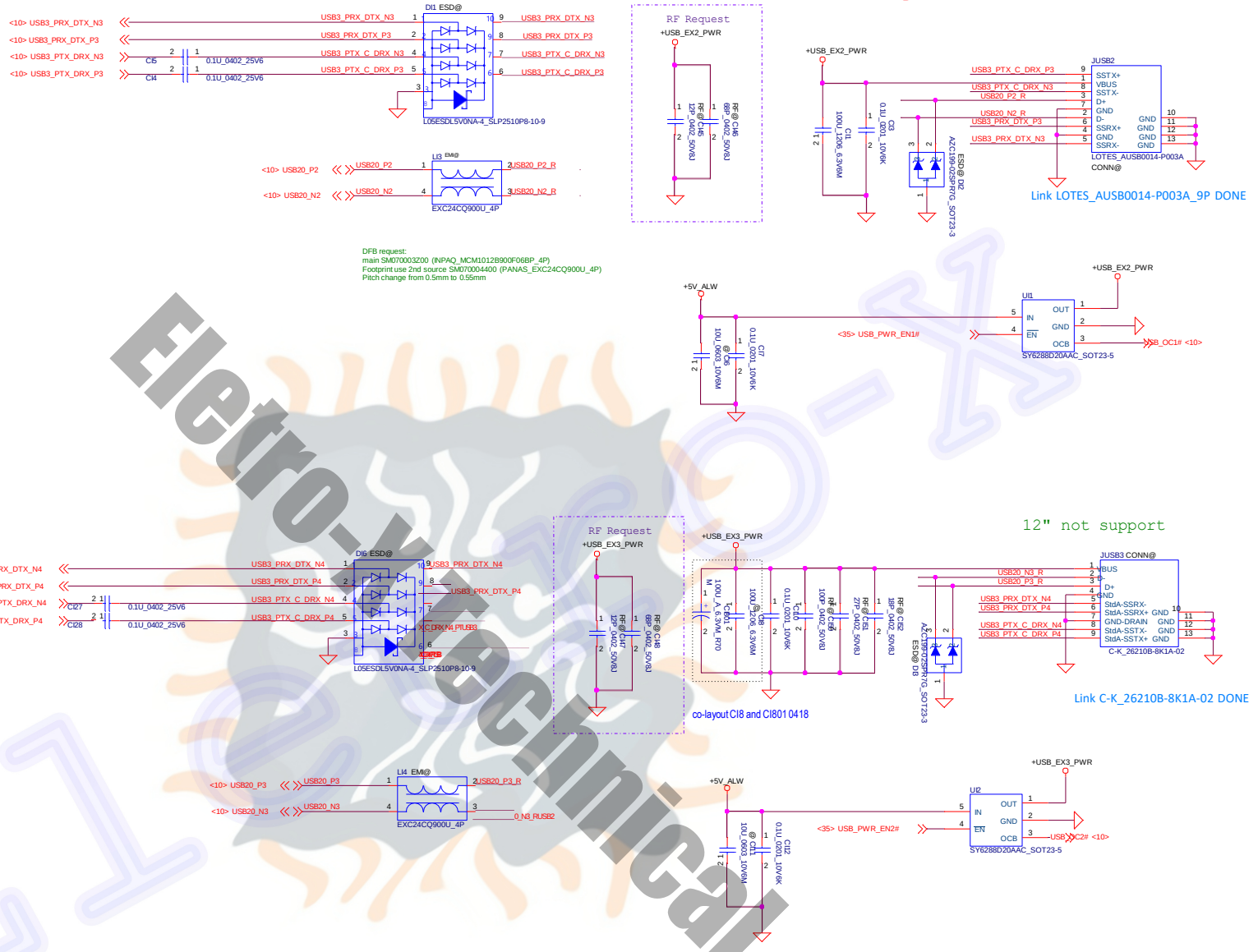
DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.

Title	JUSB1+PS	
Size	Document Number	LA-F402P
Date: Friday, August 17, 2018		Sheet 43

Eletro-X



Eletro-X Technical

DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.

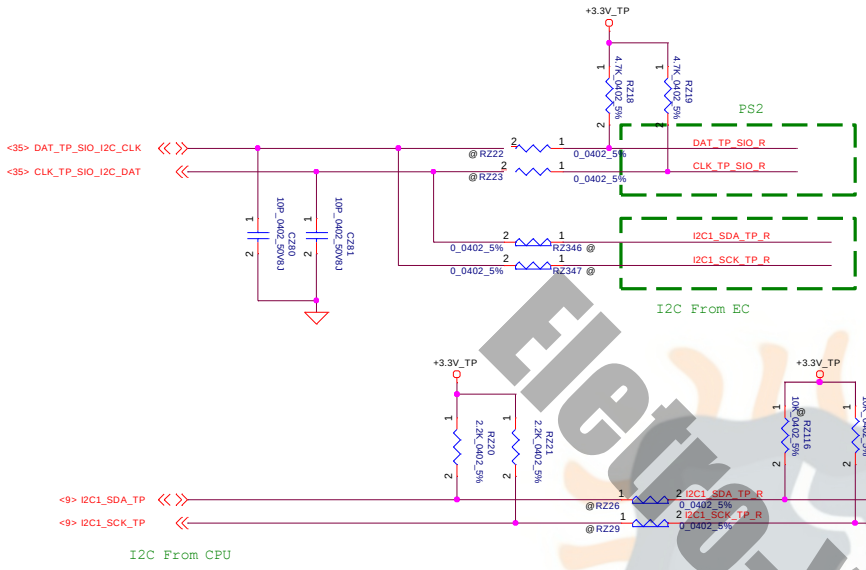
Title: JUSB2&JUSB3

Size: | Document Number: LA-F402P | Rev:

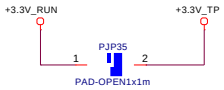
Date: Friday, August 17, 2018 | Sheet 44

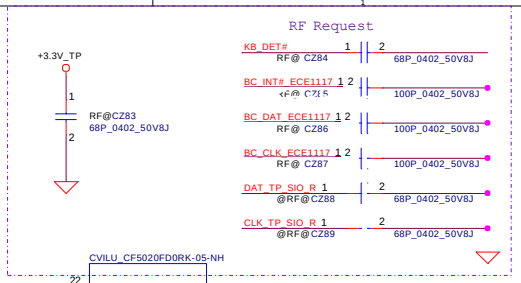
Eletro-X

Touch Pad

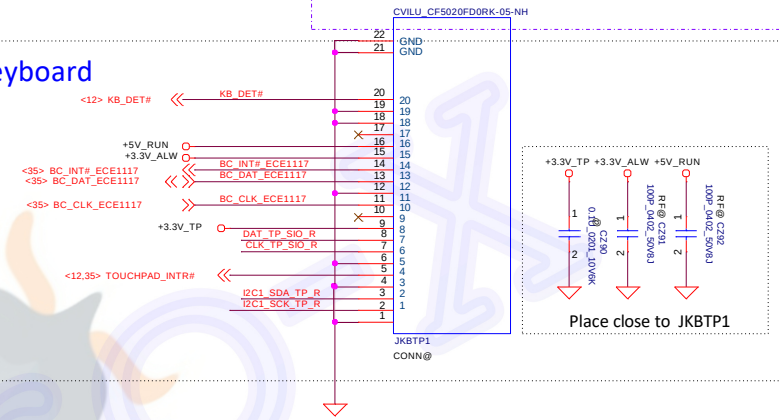


Plan is for I2C to be driven by the EC for Win7 and Pre-OS (will utilize Intel I2C drivers for Win7)
For Win8.1 and 10 the EC will control TP over I2C Pre-OS and then the PCH will drive I2C when in Windows
Route PS2 from EC to the touch pad also for contingency plan if I2C has issues



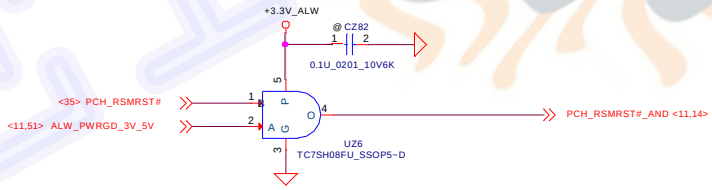


Keyboard



Link HRS_TF49-20S-0P5SH done

RSMRST circuit



DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.

Title: Keyboard

Size: | Document Number: LA-F402P

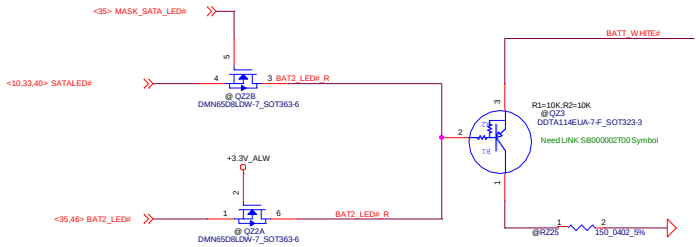
Date: Friday, August 17, 2018 | Sheet 45

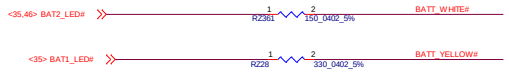
Eletro-X Technical

Battery LED

HDD LED MUX

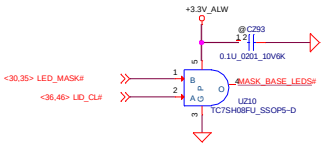
means EC can switch battery white led and HDD LED by hot key ¡§Fn+Hj¨



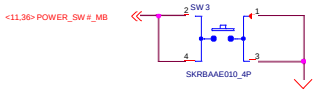


Breath LED

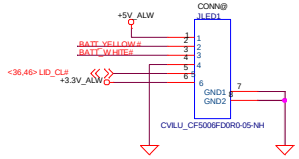
LED P/N change to SC50000FL00 from SC50000BA00



POWER & INSTANT ON SWITCH



LED board CONN



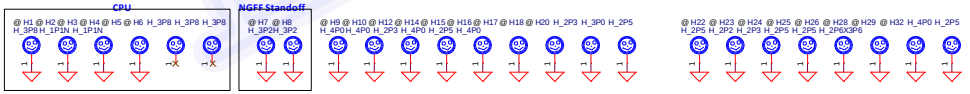
Link CF5006FD0R0-05-NH DONE

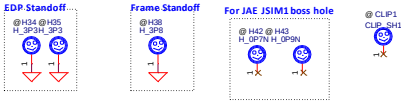
Fiducial Mark

@FD1 FIDUCIAL MARK~D
@FD2 FIDUCIAL MARK~D
@FD3 FIDUCIAL MARK~D
@FD4 FIDUCIAL MARK~D

LED Circuit Control Table

	LED_MASK#	LID_CL#
Mask All LEDs (Unobtrusive mode)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1





DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.

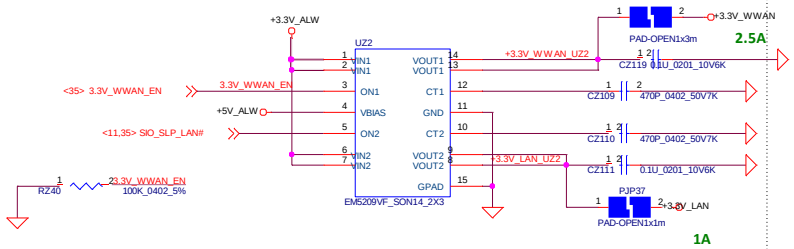
Title: PAD, LED

Size: | Document Number: LA-F402P | Rev: 0.2

Date: Friday, August 17, 2018 | Sheet: 37 of 41

Eletro-X Technical

+3.3V_WWAN/+3.3V_LAN source

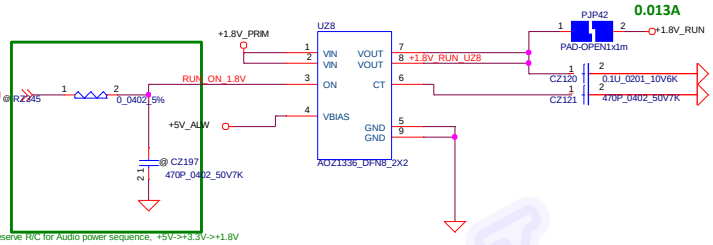


+3.3V_WWAN_UZ2

RF@ CZ124 2200P_0402_50V7K

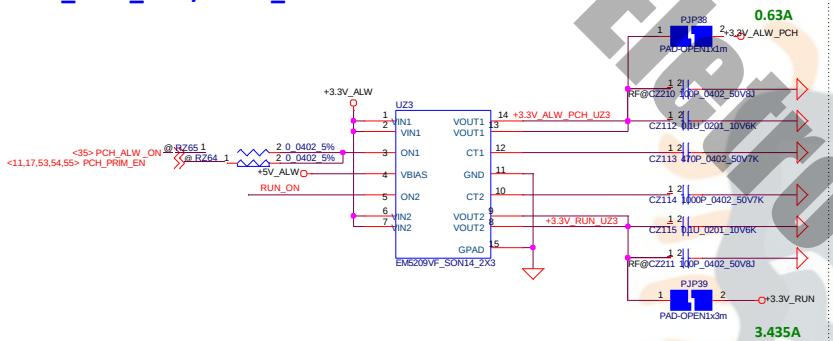
RF Request

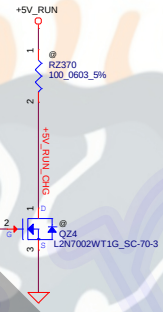
+1.8V_RUN source



Reserve R/C for Audio power sequence, +5V->+3.3V->+1.8V

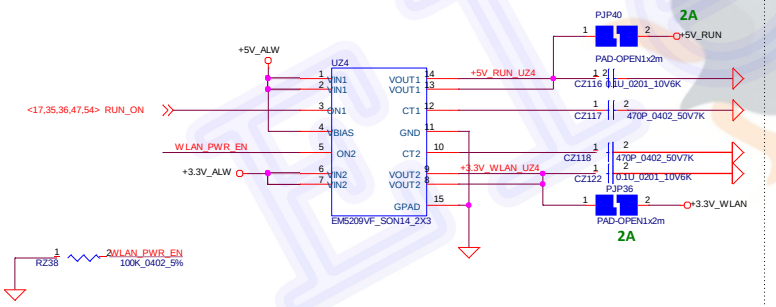
+3.3V_ALW_PCH/+3.3V_RUN source

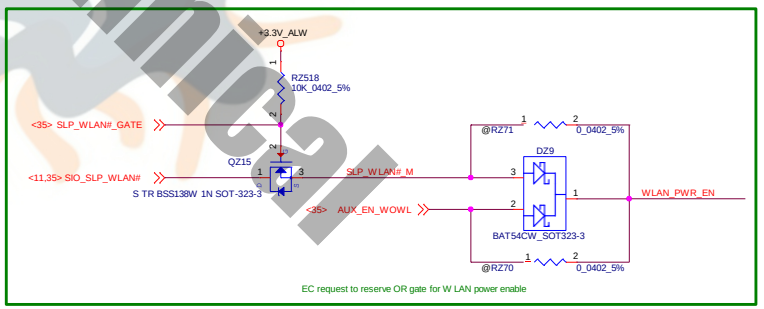




Reserve for S3 no power issue (+5V_RUN discharge circuit)

+5V_RUN/+3.3V_WLAN source





EC request to reserve OR gate for W LAN power enable

DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

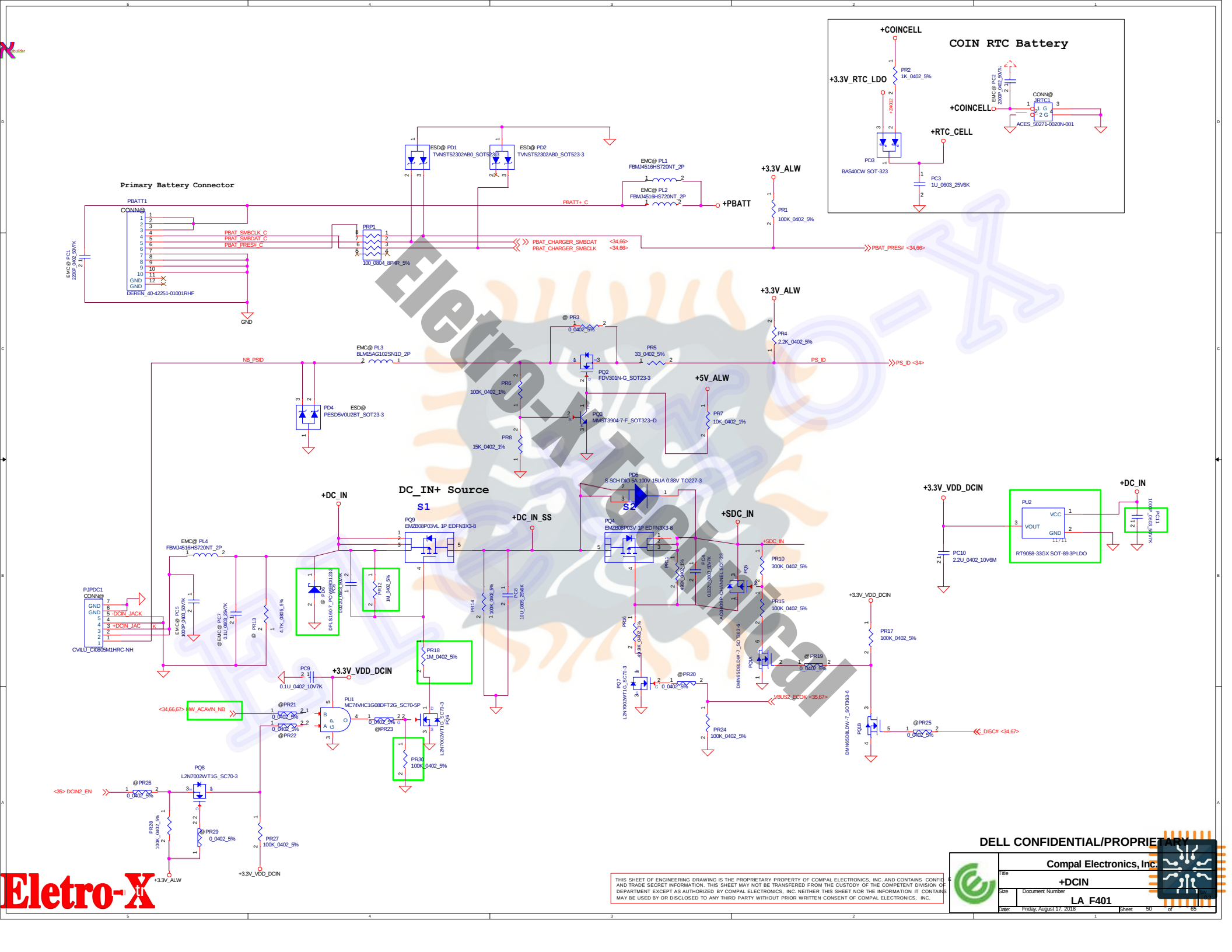
Compal Electronics, Inc.

Title: Power control

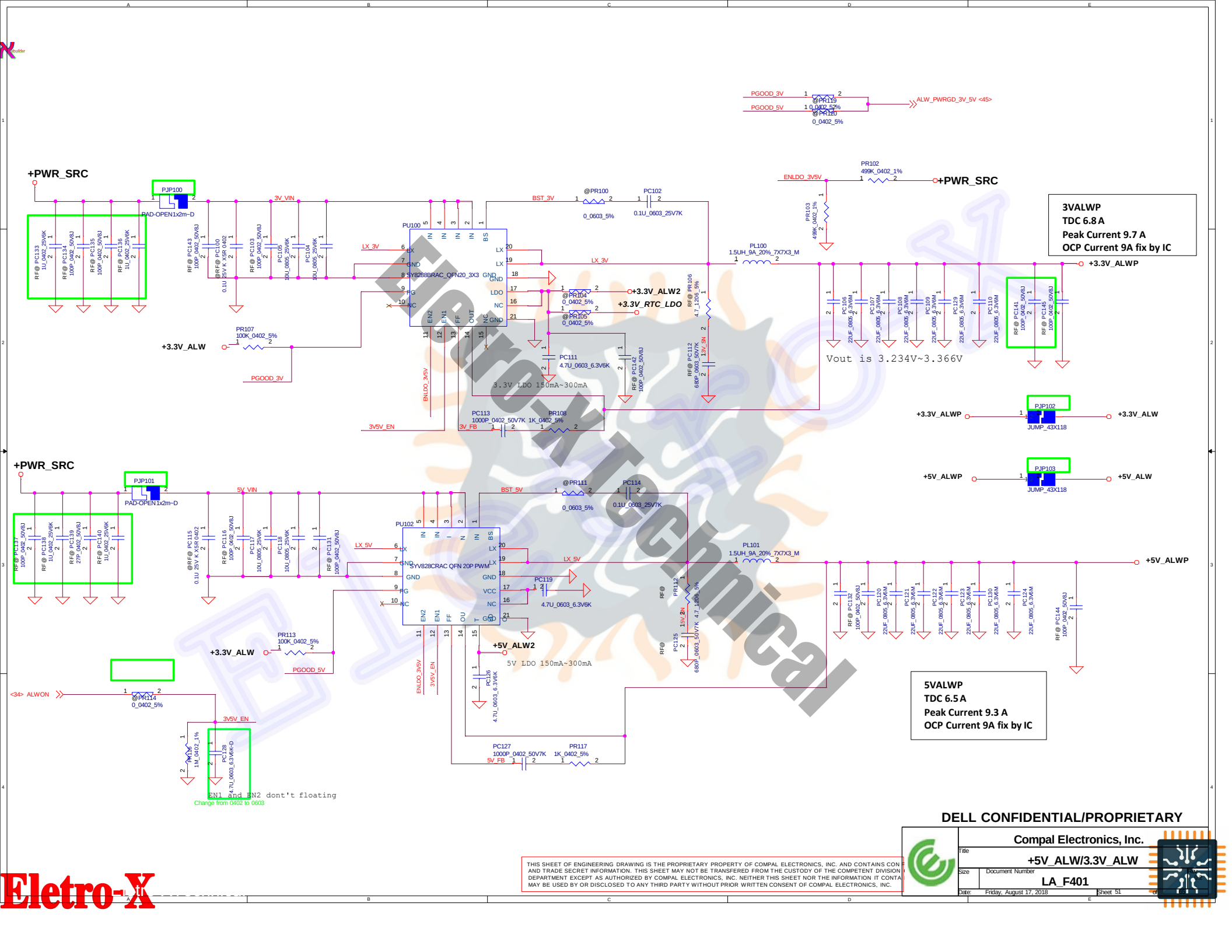
Size | Document Number: LA-F402P | Rev

Date: Friday, August 17, 2018 | Sheet 47

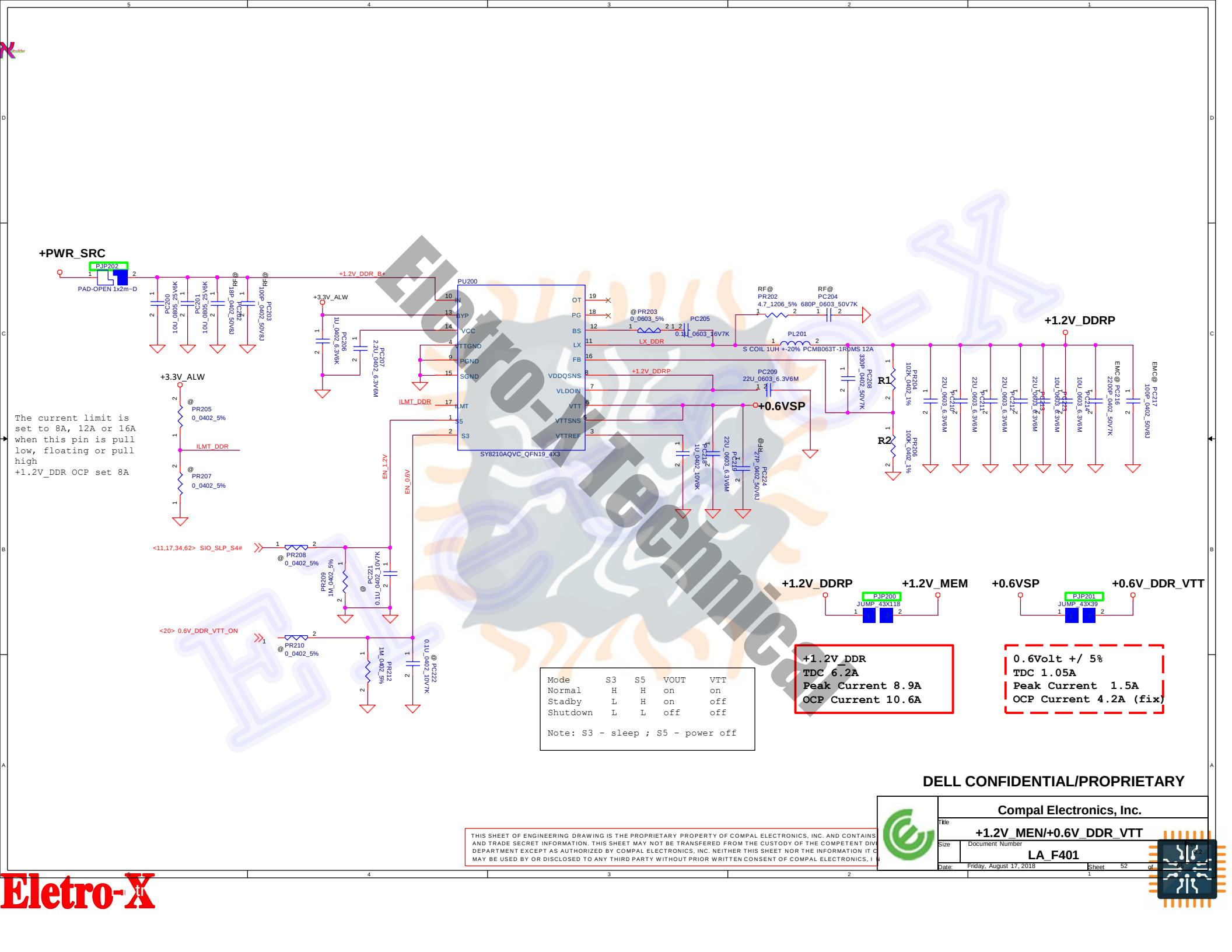
Eletro-X Technical



Eletro-X Technical



THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CON
AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION
DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTA
MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.



Eletro-X Technical

DELL CONFIDENTIAL/PROPRIETARY

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS
AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIV
DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT C
MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, I

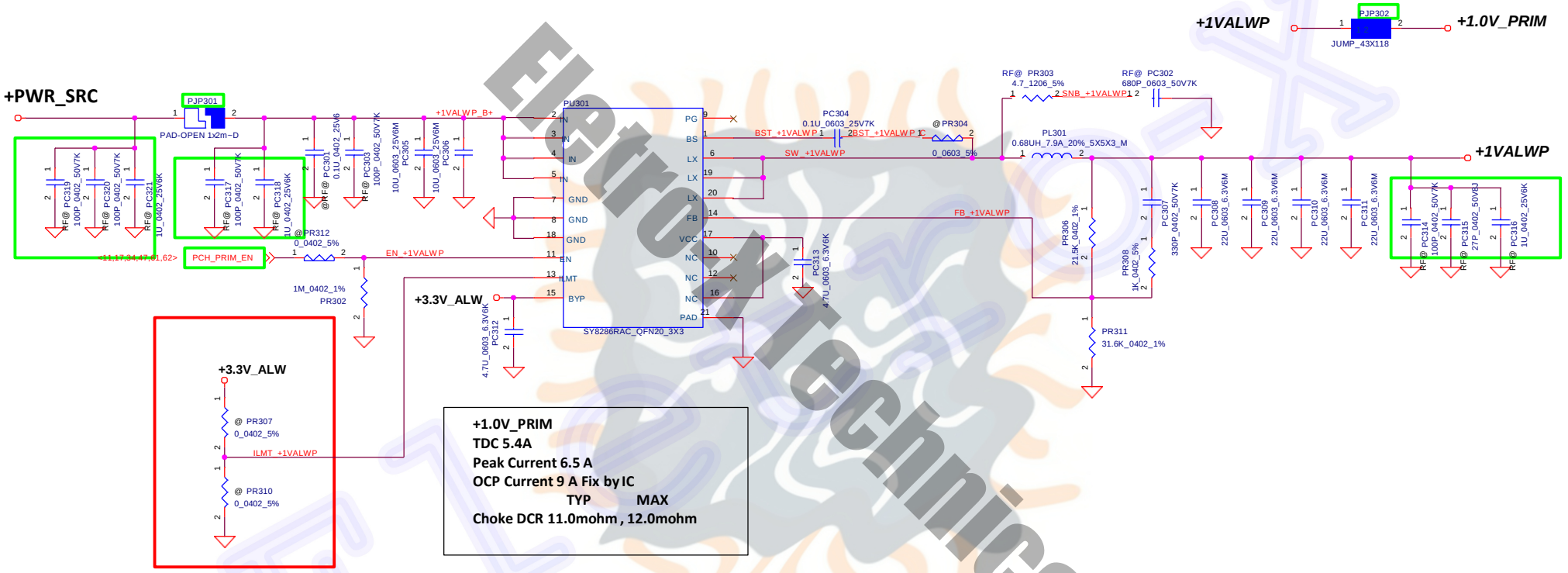
Compal Electronics, Inc.

Title: +1.2V_MEN/+0.6V_DDR_VTT

Size | Document Number: LA_F401

Date: Friday, August 17, 2018 | Sheet 52 of

Eletro-X



The current limit is set to 6A, 9A or 12A when this pin is pull low, floating or pull high

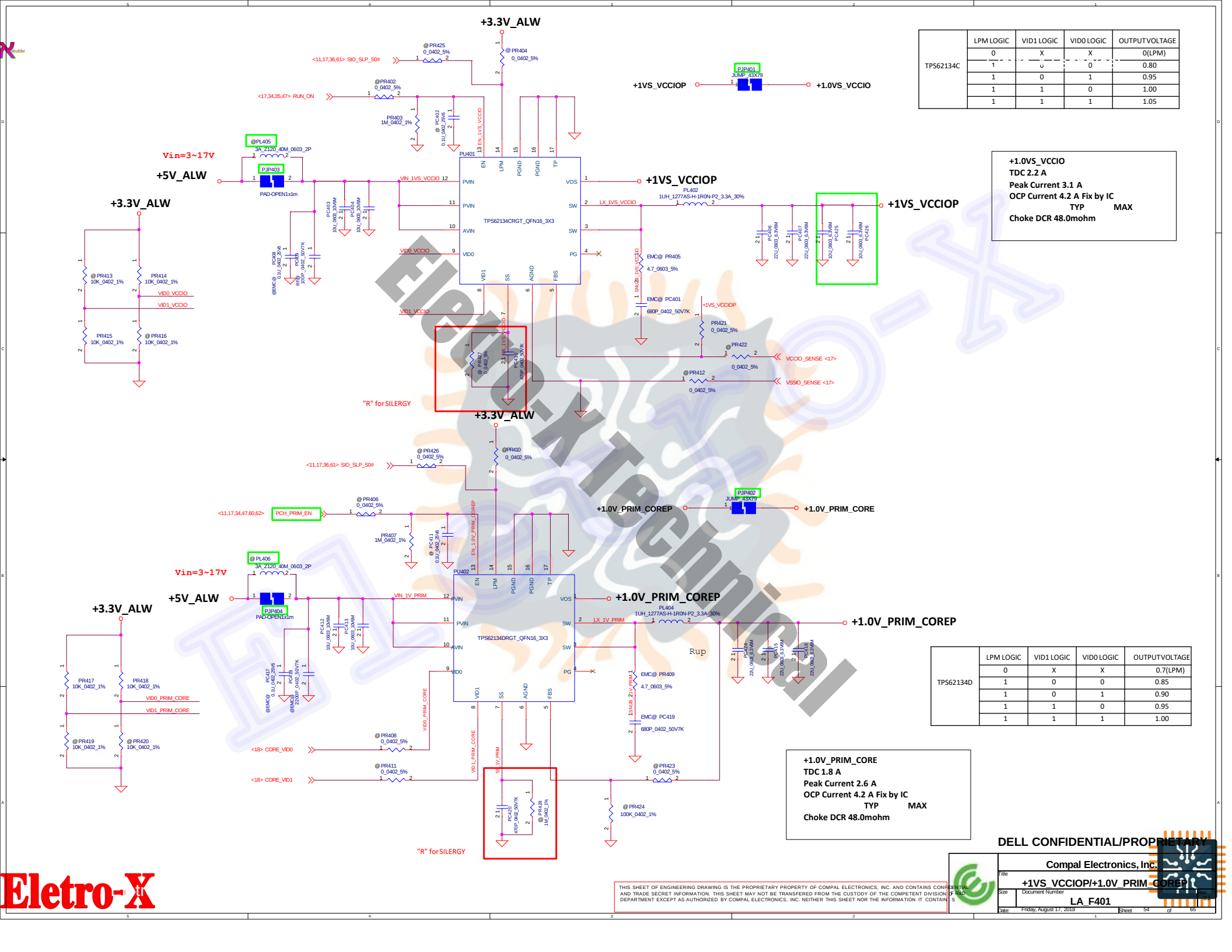
Eletro-X Technical

DELL CONFIDENTIAL/PROPRIETARY

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS C
AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVI
DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT C

Compal Electronics, Inc.	
Title	+1VALWP
Size	Document Number: LA_F401
Date: Friday, August 17, 2018	Sheet 53 of

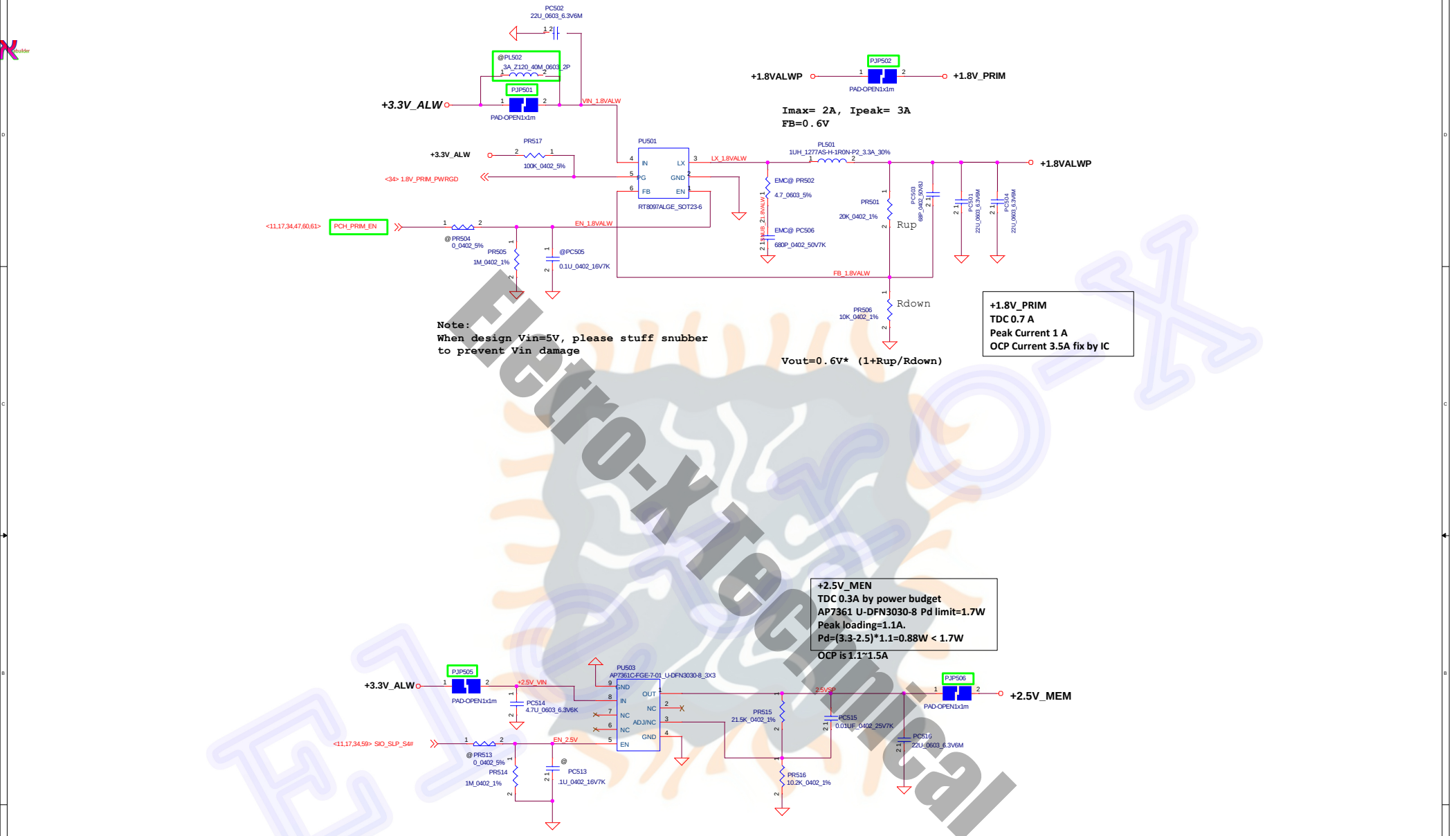
Eletro-X



TPS62134C	LPM LOGIC	VID1 LOGIC	VID0 LOGIC	OUTPUTVOLTAGE
	0	X	X	0(LPM)
	1	0	0	0.80
	1	0	1	0.95
	1	1	0	1.00
	1	1	1	1.05

TPS62134D	LPM LOGIC	VID1 LOGIC	VID0 LOGIC	OUTPUTVOLTAGE
	0	X	X	0.7(LPM)
	1	0	0	0.85
	1	0	1	0.90
	1	1	0	0.95
	1	1	1	1.00

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS



Eletro-X Technical

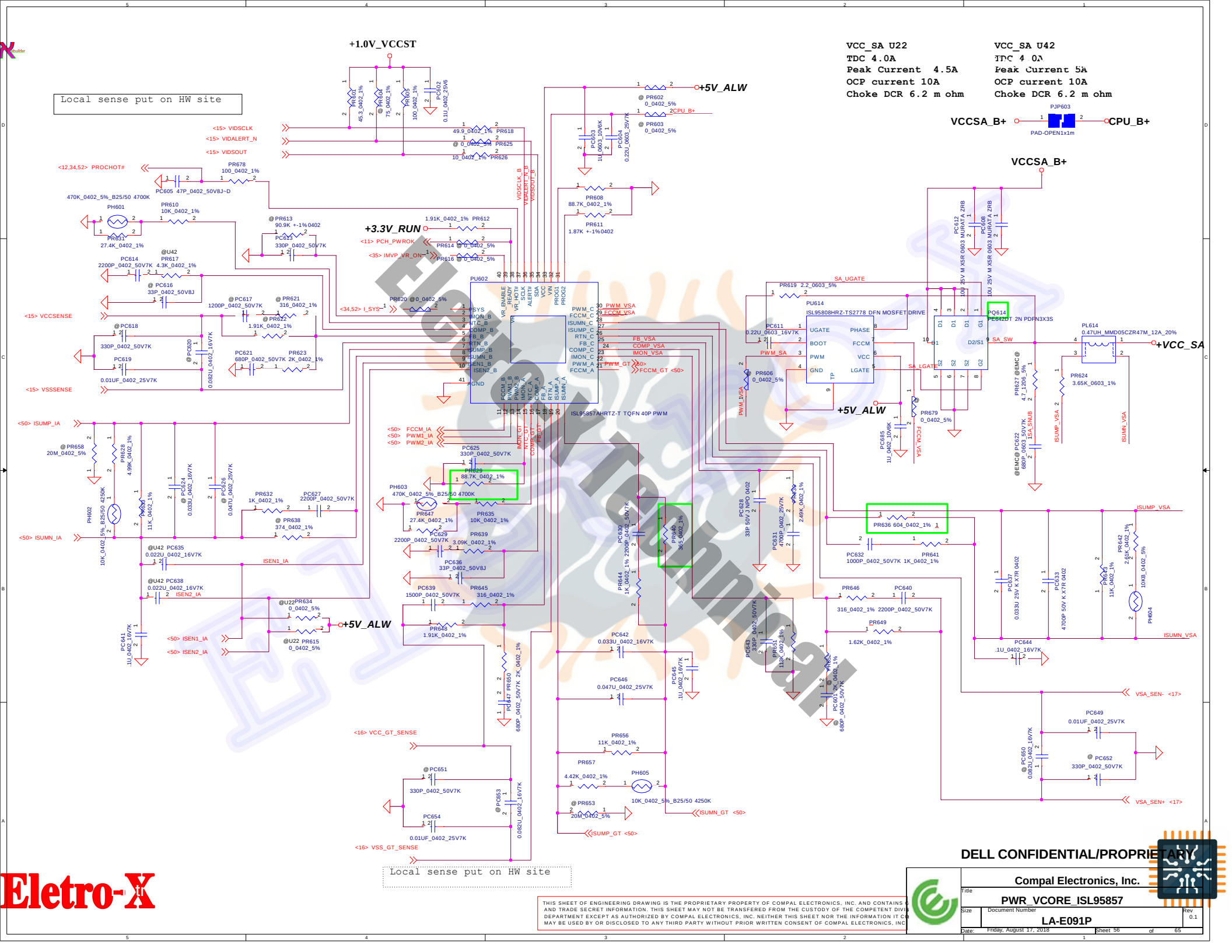
DELL CONFIDENTIAL/PROPRIETARY

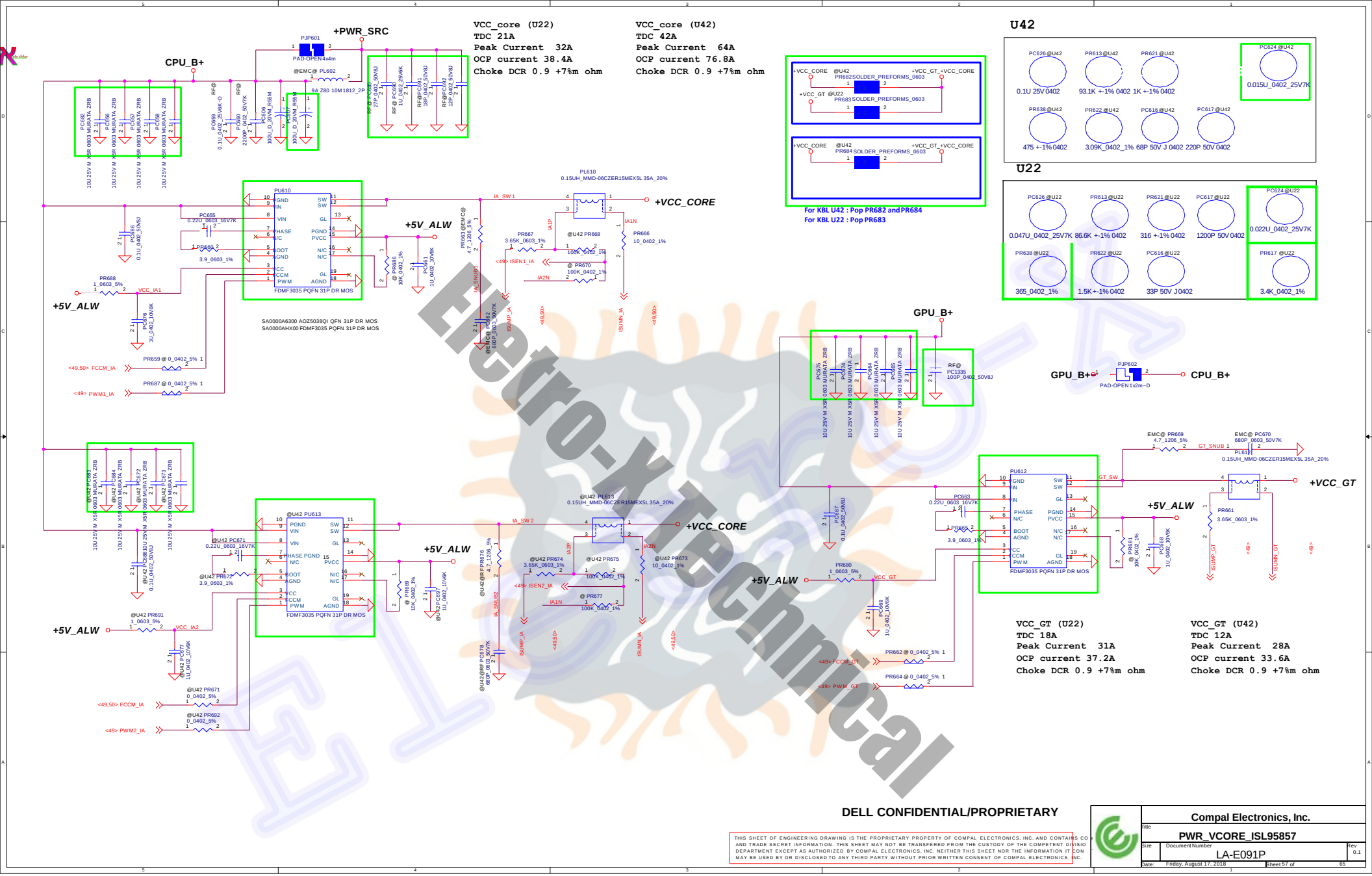
Compal Electronics, Inc.

Title	+1.8VALWP/2.5V_MEM	
Size	Document Number	Rev
	LA_F401	1.0
Date: Friday, August 17, 2018	Sheet 55 of 65	

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS

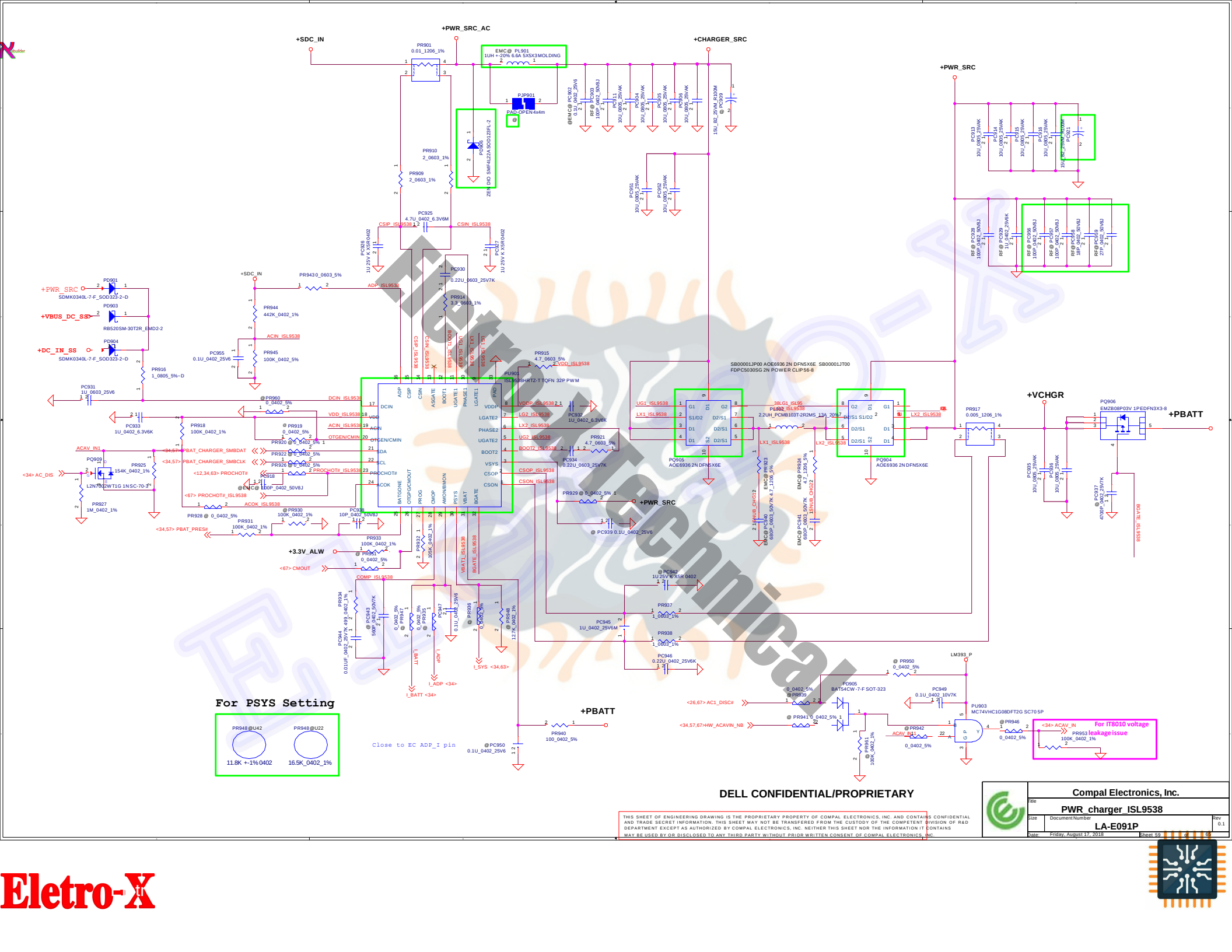
Eletro-X

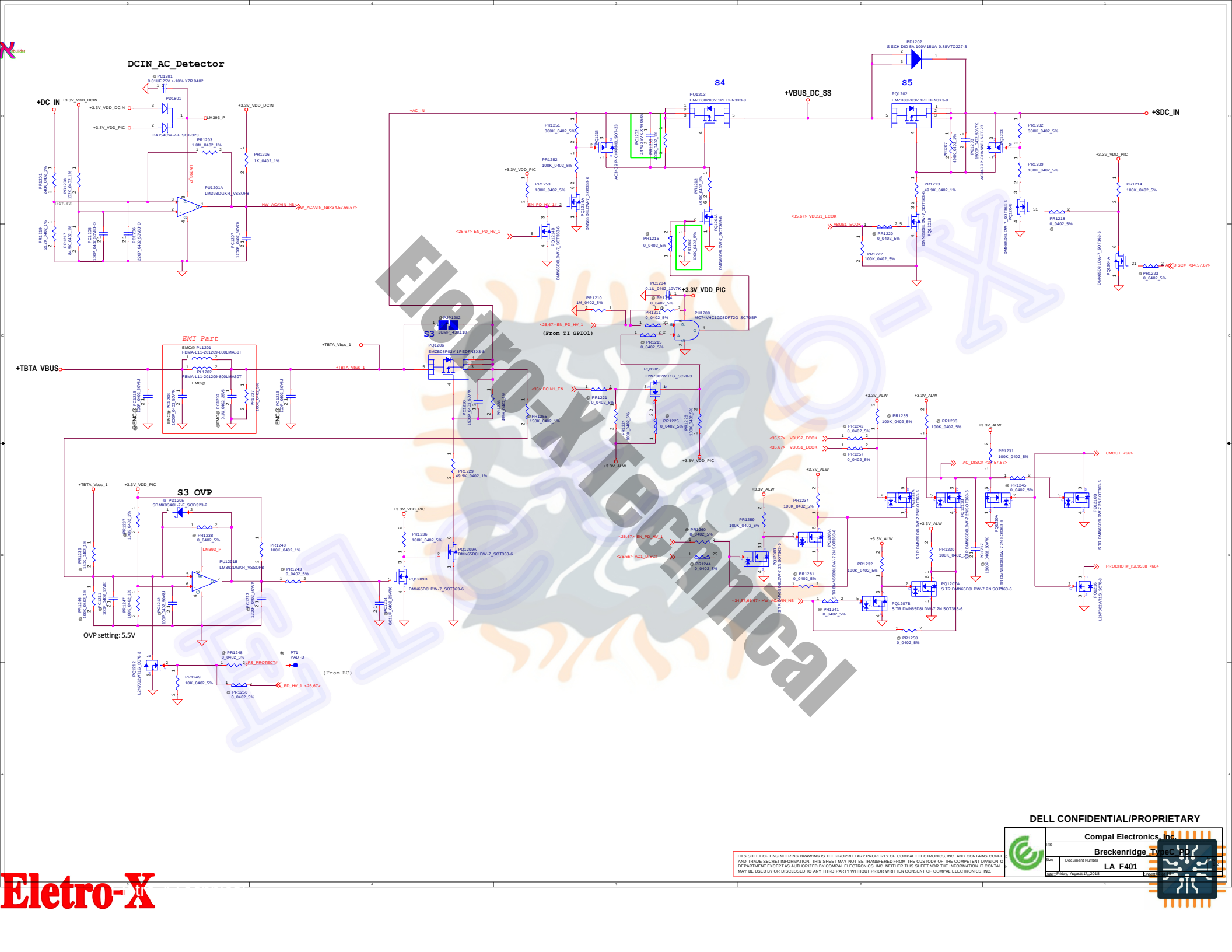

Local sense put on HW site
+1.0V_VCCST
VCC_SA U22
TDC 4.0A
Peak Current 4.5A
OCP current 10A
Choke DCR 6.2 m ohm
VCC_SA U42
TDC 4.0A
Peak Current 5A
OCP current 10A
Choke DCR 6.2 m ohm
VCCSA_B+
PJP603
PAD-OPEN1x1m
CPU_B+
+5V_ALW
+3.3V_RUN
PU602
ISL95857AHRTZ-T TQFN 40P PWM
PU614
ISL95808HRZ-TS2778 DFN MOSFET DRIVE
PQ614
PE6420T 2N PDFN3X3S
PL614
0.47UH_MMD05CZR47M_12A_20%
+VCC_SA
Local sense put on HW site
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
PWR_VCORE_ISL95857
LA-E091P
Rev 0.1
Friday, August 17, 2018
Sheet 56 of 65
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS C
AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVI
DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CO
MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.
Eletro-X Technical



Eletro-X Technical

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CO
AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISIO
DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CON
MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.


+SDC_IN
+PWR_SRC_AC
+CHARGER_SRC
+PWR_SRC
+VCHGR
+PBATT
+3.3V_ALW
ISL9538HRTZ-T TQFN 32P PWM
SB00001JP00 AOE6936 2N DFN5X6E SB00001JT00 FDPC5030SG 2N POWER CLIP 5X6-8
PQ905 AOE6936 2N DFN5X6E
PQ904 AOE6936 2N DFN5X6E
PQ906 EMZB08P03V 1PEDFN3X3-8
PQ901 SDMK0340L-7-F_SOD323-2~D
PQ903 RB520SM-30T2R_EMD2-2
PQ904 SDMK0340L-7-F_SOD323-2~D
PQ905 BAT54CW -7-F SOT-323
PU903 MC74VHC1G08DFT2G SC70 5P
PU901 ISL9538HRTZ-T TQFN 32P PWM
For PSYS Setting
PR948@U42
PR948@U22
11.8K +-1% 0402
16.5K_0402_1%
Close to EC ADP_I pin
For IT8010 voltage leakage issue
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
PWR_charger_ISL9538
LA-E091P
Friday, August 17, 2018
Sheet 59 of 69
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.


DCIN_AC_Detector
+DC_IN
+3.3V_VDD_DCIN
+3.3V_VDD_PIC
PD1801
BAT54CW-7-F SOT-323
LM393_P
PU1201A
LM393DGKR_VSSOP8
HW_ACAVIN_NB
HW_ACAVIN_NB<34,57,66,67>
+AC_IN
S4
S5
+VBUS_DC_SS
+SDC_IN
PQ1213
EMZB08P03V 1PEDFN3X3-8
PD1202
S SCH DIO 5A 100V 15UA 0.88VTO227-3
AO3419 P-CHANNEL SOT-23
DMN65D8LDW-7_SOT363-6
EN_PD_HV_1
<26,67> EN_PD_HV_1
<35,67> VBUS1_ECOK
VBUS1_ECOK_1
S3
JUMP_43X118
(From TI GPIO1)
PU1200
MC74VHC1G08DFT2G SC70SP
PQ1205
L2N7002WT1G_SC70-3
<35> DCIN1_EN
EMI Part
+TBTA_VBUS
+TBTA_Vbus_1
EMC@ PL1201
FBMA-L11-201209-800LMA50T
PL1202
S3 OVP
PD1205
SDMK0340L-7-F SOD323-2
PU1201B
LM393DGKR_VSSOP8
OVP setting: 5.5V
PQ1209A
PQ1209B
DMN65D8LDW-7_SOT363-6
PQ1212
PQ1207A
PQ1207B
S TR DMN65D8LDW-7 2N SOT363-6
PQ1208A
PQ1208B
PQ1217
PQ1218
PQ1204A
PQ1204B
PQ1203
PQ1206
EMZB08P03V 1PEDFN3X3-8
AC_DISC# <34,57,67>
CMOUT <66>
PROCHOT#_ISL9538 <66>
VBUS2_ECOK
VBUS1_ECOK
HW_AC_DIN_NB
ALS_PROTECT#
PT1
PAD-D
(From EC)
PD_HV_1 <26,67>
AC1_DISC#
EN_PD_HV_1
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
Breckenridge_TypeC_PD
LA_F401
Friday, August 17, 2018
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFI
AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION O
DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTA
MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

VCC_CORE Place on CPU
22U_0603 * 33 pcs +1U_0201*31 pcs
+330u_D7*3 pcs

VCC_GT Place on CPU (U22)
22U_0603 * 19 pcs +1U_0201*14 pcs
+330u_D7*2 pcs

+VCC_CORE

+VCC_GT

+VCC_SA

+VCC_GT_+VCC_CORE

VCC_SA Place on CPU
22U_0603 * 12 pcs + 1U_0201*7 pcs

VCC_GT_+VCC_CORE Place on CPU
22U_0603 * 6 pcs + 1U_0201*5 pcs

Eletro-X Technical

DELL CONFIDENTIAL/PROPRIETARY

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CO
AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISIO
DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CON
MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.		
Title: PROCESSOR DECOUPLING		
Size	Document Number: LA-E111P	Rev
Date: Friday, August 17, 2018	Sheet 58	of

Eletro-X

tfersion Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	57	Change DrMOS	2017 06/07	Compal	Change DrMOS from TI to Fairchild	1. DrMOS change from CSD97396 to FDMF3035 2. PR660, PR672, PR665 Change from 2.2R to 3.9R 3. Remove PC679, PC680, PC681 4. PC686, PC687, PC688 change from 10P to 0.1U	X01
2	51 57 59	Add EMI portion	2017 06/09	Compal	EMI request & modify Components	1. Depop PC133, PC134, PC135, PC136, PC137, PC138,PC139,PC140, PC689, PC690, PC691, PC692, PC956, PC957,PC958, PC959 2. Pop PL901.	X01
3	53 54 56 57	Add RF team portion	2017 06/13	Compal	RF request & modify Components	Pop PC622,PR627, PC401, PR405, PC419, PR409, PC506, PR502, PC409, PC303	X01
4	56 57 59	Acoustic solution	2017 06/13	Compal	For acoustic solution CPU input MLCC change to 0603 low noise MLCC	1. Remove PC917, PC918, PC919, PC920 , add PC921 B2 POS CAP 2. CPU input MLCC size change from 0805 to 0603 low noise MLCC PC608, PC612, PC656, PC657, PC658, PC664, PC665, PC672, PC673, PC674, PC675, PC682, PC683, PC684 3. Pop PC607	X01
5	59	Change Charger DualMOS	2017 06/13	Compal	Change DualMOS from TI to AOS	DualMOS change from CSD87351 to AOE6936	X01
6	57~ 76	MLCC	2017 07/31	Compal	LD request to change cap to 0end P/N	0end P/N for all cap	X02
7	66	EMI		Compal	EMI request	TpyeC PD Bead EOL ,so change BR_MLK12_14_15 PL1201/PL1202 Bead to 80 ohm bead, CPN:SM01000P200„»SM01000U300(2nd) CPN:SM01000P200„»SM01000U400(main)	X02
8	57 65 66	2nd source		Compal	HW request for 2nd source list change	For Main source SA00000OH00 , 2nd source change SA007080100 ¡÷ SA741080400	X02
9	65	chager resister		Compal	Charger current sense resister derating	PR937,PR938,PR909,PR910,PR915 0402>0603 SD014100B80 S RES 1/10W 1 +1% 0603 PR937,PR938 SD00001QK00 S RES 1/10W 2 +1% 0603 PR909,PR910 SD013470B80 S RES 1/10W 4.7 +5% 0603 PR915	X02
10	57~ 76	0 ohm shortpad		Compal	0hom change to 0 ohm short pad	For 0ohm no short pad: Keep PR943,PR421,PR671,PR692 pop SD028000080	X02
11	65	chager		Compal	For adapter plugin bouncing issue	Add PD906 SC40000EL00(S ZEN DIO SMF4L22A SOD123FL2) before PL901 Isum choke	X02
12	65	chager		Compal	Buyer request	PD901,PD904 change from SCS0340L010 to SCS00009P00, for common part	X02
13	58 63	RF portion		Compal	RF request	Add MLCC for RF 100P_0402_50V: PC1335 PC141 PC142 PC143 PC314 PC317 PC144 PC145 PC319 PC320 27P_0402_50V:PC315 PC224 1U_0402_50V: PC316 PC318 PC321	X02
14							

DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.

Title: PWR P.I.R

Size: Document Number: LA_F401

Date: Friday, August 17, 2018 Sheet

Eletro-X Technical

tfersion Change List (P. I. R. List)

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
15							
16							
17							
18							
19							
20							
21							
22							
23							
24							
25							

Eletro-X Technical

DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.

Title: PWR P.I.R

Size | Document Number: LA_F401 | Rev: 0.2

Date: Friday, August 17, 2018 | Sheet 62 of 68

Eletro-X

tfersion Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	40	M2 2280 Socket	2017/03/9	EE	For align with spindle HDD.	Add UZ37 circuit for 2280 SSD imdenpenden loadswitch > add CN50~51, UZ37, PJP30_1*2(and no stuff all)	0.1(X00)
2	All	All	2017/03/9	EE	X9 request	UC1 CPU change from U22 to U42.	0.1(X00)
3	11	CPU (6/14)	2017/03/14	EE	KBLR U42 X'tal	Add RC417~RC422,CC334,CC335, YC3 for U42 crystal	0.1(X00)
4	34	USH & TPM	2017/03/17	EE	Prevent POA_WAKE# ESD	Add RZ364 100 ohm to POA_WAKE#	0.1(X00)
5	All	All	2017/03/17	EE	Remove IO expander	11.Delete expander IO UE2 relating circuit(RE524,@RE525 change to 0 ohm) remove UE2, CE1, CE2, RE13~18, RE6, CE500, CE504, CE505 4/13 add UMA RE524/525(2.2kohm)> B6/F7 4/17 B6/F7 change netname to GPU_SMDAT/CLK 12. GPIO change (RE374 reserve) PCH_RSMRST#_GPIO204 > USH_PWR_STATE# (delete RE363) PORT80_DET# > DCIN1_EN (delete RE512,RE513,RZ131) SHD_IO3 > VBUS1_ECOK (delete RE366~RE373, RE376,RE377,RE98,UE9) SHD_IO1 > SATA_LED_EN ENVDD_PCH > DCIN2_EN SIO_RCIN#_EC > VBUS2_ECOK 13 For DSC (keep RE524, RE525)change name GPU_SMDAT/GPU_SMCLK SIO_EXT_SCI#_EC > GPU_PWR_LEVEL (delete RE341) EXPANDER_GPU_SMCLK > DGPU_PWROK RTCRST_ON_GPIO141(B6) > GPU_SMDAT X(F7)> GPU_SMCLK	0.1(X00)
6	36	MEC5105 Support	2017/03/24	EE	Remove Reset Threshold circuit	1. Delete UE7 relating circuit. keep RE536 only remove UE7, QE13, RE34, RE348, RE536, RE537, RE530 CE5, CE6, CE503 add RE536 on EC side	0.1(X00)
7	All	All	2017/03/24	EE	Add RTC reset circuit	1. RTCRST_ON_GPIO122 change to RTCRST_ON... 21. +RTC_CELL_PCH circuit (Dell request) Delete RE514,RE515... Add QE14~QE17... Add RE540~RE546... Add CE63... Change RC56.2 net name to +RTC_CELL_PCH... Change UC1.AK19, UC1.BB14 net name to +RTC_CELL_PCH... 22.based on ARD1.3 ¥[¦^iRTC circuit¼W¥[RE551Ã×§K+RTC_CELL_PCH¨S¹q. 3. +3.3V_ALW_DSW enable circuit (Dell request) Delete RE524... Add RC431~RC433... Add UC13,UC14... Change UE1.M7 net name to VCCDSW_EN_GPIO... 4. GPIO change USH_SMBCLK > USH_EXPANDER_SMBCLK USH_SMBDAT > USH_EXPANDER_SMBDAT Delete RTCRST_ON_GPIO141 PRIM_PWRGD_GPIO024 > RESET_IN# 5.UC13 chante to QC6, UC14 change to QC7 4/17 RTC power Gate circuit rev.2 Delete RE540, RE542, RE544, RE545, QE14, QE16 Change RE543 to 1M ohm and RE546 to 10K ohm	0.1(X00)
						Add DE2, CE65, Reserve CE66 for VCCDSW_EN	

DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.

Title: EE P.I.R (1/7)

Size: | Document Number: LA-F402P | Rev:

Date: Friday, August 17, 2018 | Sheet 63

Eletro-X Technical

Eletro-X

tfersion Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
8	All	All	2017/03/14	EE	colay DS3/nonDS3	1. DS3 / nonDS3 colay Add DC2, (DC1 add NDS3 @) Add RC501, RC503, RC505 for DS3 Add RC502, RC504, RC506 for NonDS3 Use the original 0ohm, RC215 instead of RC504, RE536 instead of RC503 3/14 1. based on EDS that add RC503 / RC504 on SUSACK # / ME_SUS_PWR_ACK for DS3 2. UZ3 enable pin change netname to PCH_PRIM_EN 3. RE349 + DS3 @ 4. UZ234 input in form SIO_SLP_SUS # to PCH_PRIM_EN 3/15 1. For align KW that change as below "Part Reference" A RC501 > RC439 B. RC502 > RC440 C. RC503 > RC443 D RC504 > RC444 E. RC505 > RC441 F RC506 > RC442 3/27 Parallel 0ohm in DC2, reserved to avoid NDS3 @, EC too late to load code	0.1(X00)
9	09	CPU (4/14)	2017/03/27	EE	For antenna request	4/17 RC Power Gate Circuit Option 1. Add RC434 ,RC435 0ohm for JUART1 power option RC445 change to connect to VCC_DSW_EN and pop 4/1 JUART1 wether pin swap, Align with SB. > Pin swap align SB > EVT phase pop JUART, DVT phase remove 4/20 2. Remove RC435	0.1(X00)
10	38	USH & TPM	2017/03/27	EE	Prevent contactless_det# backdrive	1. Add DZ8 to prevent contactless_det# backdrive	0.1(X00)
11	37	USH & TPM	2017/03/15	EE	TPM650 include	1. TPM a. Delete RZ113, RZ111, QZ9 b. Add RZ365 and connect to +UZ12_TPM Add RZ366 and connect to +3.3V_M_TPM	0.1(X00)
12	13	CPU (8/14)	2017/03/15	EE	Follow CRB	UC1.F65 & G65 to GND add RC436 to GND before UC1.F65 & G65	0.1(X00)
13	16	CPU (11/14)	2017/03/15	EE	Follow MOW08	UC1.K52/AK52 Must be NOT connected	0.1(X00)
14	10	CPU (5/14)	2017/03/28	EE	X9 Port MAP check	1. USB3.0 port1 with port6 swap 2. USB2.0 port1 with port9 swap	0.1(X00)
15	9	CPU (4/14)	2017/03/29	EE	For Layout power trace	add +UART1_R power netname on JUART1	0.1(X00)
16	8	CPU (3/14)	2017/03/29	ME	Connector check	JSPI1 change from ENTERY_SP01001FW00 to ACES_SP01001CB10	0.1(X00)
17	31,11	Card Reader RTS5242 CPU (6/14)	2017/03/29	EMI	EMI request	1. RR5~RR10 change to 0ohm 2. RC417~RC420 change from 0ohm to 33ohm	0.1(X00)
18	28	USB 3.0 CONN TYPE C	2017/03/29	ESD	ESD request	1. Change DT7, DT8, DT11, DT12 to DT39 2. Change DT15, DT16, DT19, DT20 to DT40	0.1(X00)

Eletro-X Technician

DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.

Title: EE P.I.R (2/7)

Size: | Document Number: LA-F402P | Rev:

Date: Friday, August 17, 2018 | Sheet 64

Eletro-X

tfersion Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
19	16	CPU (11/14)	2017/03/29	EE	For BRMLK12 layout request	Let AK70,BB57,BB66,AU58,AU63 flooting	0.1(X00)
20	All	All	2017/03/31	EE	Follow ARD1.3 remove WIGIG	11.change Source 1:3 demultiplexer(PS8348B) to 1:2 demultiplexer(PS8338B) 12,remove RV71, RC74, RV77, CV80 21. (DP)JNGFF1 remove CV145~150, CV152, CV153, CV156, CV157 22. (PCIE)JNGFF1 remove CZ14, CZ15 UC1 remove RC375	0.1(X00)
21	37	USH & TPM	2017/03/31	EE	TPM NPCT65X and NPCT75X schematic colay	UZ12 relating circuit and change UZ12 to SA0000AQ200	0.1(X00)
22	35	EC MEC5105	2017/04/05	EE	RTCRST_ON glitch	Reserve CE64	0.1(X00)
23	8	CPU (3/14)	2017/04/05	EE	Winbond 16MB SPI ROM EOL (change to Jdie)	Change UC5, UC6 to SA00005VV20	0.1(X00)
24	26	[Type C]PD Controller TI	2017/04/05	EE	Change PD to PD3.0	Change UT5 to SA0000AP500	0.1(X00)
25	36	MEC5105 Support	2017/04/05	EE	Board ID define change	change RE79 to 240K for X00	0.1(X00)
26	All	All	2017/04/05	EE	EC GPIO check	1. rename form AUD_NB_MUTE# to NB_MUTE# for EC team request 2. rename form SYS_LED_MASK# to LED_MASK# for EC team request 3. change net name form THERMATRIP1# to THERMTRIP1# for EC team request 4. swap WWAN_RADIO_DIS# from UE1.M2 to UE1.F12 5. swap LCD_TST from UE1.D1 to UE1.M2	0.1(X00)
27	All	All	2017/04/06	EE	EC GPIO check	1. rename form FAN1_TACH to TACH_FAN1 for EC team request 2. DSC_swap DGPU_PWR_EN to GPIO100 for save level shift at BR MLK project 3- 1. DSC_swap GPU_PWR_LEVEL to GPIO126 for save level shift at BR MLK projcet 32. DSC_ remove RE5 of GPIO126, 33. UMA_remove RE341 of SIO_EXT_SCI# 4. SYS_PWROK reserved 0ohm add netname to RESET_OUT 5. rename form ME_FW_EC to ME_FWP for EC team request rename from ME_FWP to ME_FWP_PCH 6. rename from THERMATRIP2# to THERMTRIP2# for EC team request 7.rename from HW_GPS_DISABLE# to GPS_DISABLE# for EC team request 81. rename from VGA_ID to VGA_IDENTIFY for EC team request 82. swap to GPIO035 form GPIO017 for ECteam suggestion BEEP need change to PWM function 83. Swap BEEP pin to GPIO035 form GPIO017 EC team request. 9. rename from H_PROCHOT# to PROCHOT# for EC team request 10. rename from USB_PWR_SHR_VBUS_EN to USB_POWERSHARE_VBUS_EN for EC team request	0.1(X00)
28	47	Power control	2017/04/07	EE	+5V_RUN discharge circuit for S3 no power issue	1. Add bill of stuff QZ4 and RZ370 2. Add zener diode DE1 (no stuff) for + 5V_RUN discharge 3. RZ370 into 0603 packaging, add net name	0.1(X00)
29	8	CPU (3/14)	2017/04/07	ME	JSPI1 footprint pin1 Reversal 180 of ENTERY to ACES	Symbol reverses 180 degrees	0.1(X00)
30	24	DP to VGA & VGA Conn	2017/04/07	EE	When the system can not read the VGA EDID, the maximum resolution will be pressed at 1024x768	reserve RV620 PU to +3.3V_RUN ** Pop RV620	0.1(X00)
31	36	MEC5105 Support	2017/04/07	EE	To increase power current rail for each debug card	RE71 changed to SD034100A80, that change 49.9 to 10ohm current limiting resistor to smaller.	0.1(X00)

DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.

Title: EE P.I.R (3/7)

Size: | Document Number: LA-F402P | Rev:

Date: Friday, August 17, 2018 | Sheet 65

Eletro-X Technical

Eletro-X

tfersion Change List (P. I. R. List)

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
32	All	All	2017/04/07	EE	EC GPIO check	1. rename from USB_PWR_SHR_LFT_EN# to USB_POWERSHARE_EN# for EC team request	0.1(X00)
33	All	All	2017/04/10	EE	EC GPIO check	1. 3.3V_TS_EN rename to PCH_3.3_TS_EN SHD_IO0 change to 3.3V_TS_EN and delete RE366 and PU 100K RE547 Add RV323/RV324 for 3.3V_TS_EN/PCH_3.3V_TS_EN option 2. SHD_CLK > PS_ID and delete RE374 3. CLKRUN#_EC > ENABLE_DS# and delete RE337 and add RE549, RE550 4. change net name form PANEL_ID to SYSTEM_ID 5 .SIO_EXT_SMI#_EC > free and delete RE338 6. SIO_RCIN#_EC > VBUS2_ECOK and delete RE339/RC13 7. rename from SATA_LED_EN to MASK_SATA_LED# for EC team request 8.rename form FAN1_PWM_1 to PWM_FAN1 for EC team request 9.GPIO054(PS_ID) swap to GPIO056 for EC team request 10. PCH_ALW_ON keep GPIO231 and assign DCIN2_EN to GPIO107 11. EXPANDER_GPU_SMCLK > free and delete RE525 12.this pin should be change to reserved,Current EC no use PCH_ALW_ON to control +3.3V_ALW_PCH, it control by SIO_SLP_SUS# directly 13. rename from SLOT2_CONFIG_1 to NGFF_CONFIG_1 for EC team request 14. rename from ACAV_IN_NB to HW_ACAVIN_NB for EC team request 15.rename from SLOT2_CONFIG_0 to NGFF_CONFIG_0 for EC team request 16 rename from SLOT2_CONFIG_2 to NGFF_CONFIG_2 for EC team request	0.1(X00)
34	All	All	2017/04/11	EE	PCH GPIO check	1. rename from HW_ACAVIN_NB# to ACAV_IN_NB# for EC team request 2.Follow SB reserve KR_UM#net,for mouse PCIMod 3.DEL SIO_RCIN# net,for no use LPC mode 4.Follow SB reserve SIO_EXT_SCI#,for no use LPC mode 5.Rename PCH_3.3V_TS_EN from 3.3V_TS_EN 6.Follow SB reserve PCI_CLK_LPC1, for no use LPC mode 7.Follow SB reserve PME#, for no use LPC mode 8.Follow SB reserve SIO_EXT_SMI# net, for no use LPC mode	0.1(X00)
35	All	All	2017/04/11	EE	Following port MAP	LOM port to be replaced to port 4	0.1(X00)
36	All	All	2017/04/13	EMI	EMI request	change 0ohm short pad to 0ohm of as below. RC328,RT54~57,RZ56,RN99	0.1(X00)
37	All	All	2017/04/17	EE	For All of Repeater	4/17 PWD pin setting double check for all of redrive(dual, signal, USB3) 4/21 UMA 1. SATA repeater > add QN6, RN226, RN227 2.PCIE/SATA repeater > add QN7, RN228,RN229,RN230 DSC 1. PCIE/SATA repeater > add QN6, RN226, RN227	0.1(X00)
38	All	All	2017/04/17	EE	GPIO map change	4/17 PCH_3.3V_TS_EN PU +3.3V_RUN change page to QV7.2 >Add RV326 and depop RC282/RE547 for 3.3V_TS_EN/PCH_3.3V_TS_EN 1. RC443 BOM structure change to @ 2. UMA : GPIO126>GPU_PWR_LEVEL 3. Add RTCRST_ON_R net neme for QE17.2 4. Add SIO_SLP_SUS#_R net name and PU RE561 5. RC27.2>NC for CLKRUN# 6. UMA : HDD_DET#>SATAGP0 7. Remove RE360/RE364	0.1(X00)

Eletro-X Team Repair

DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.

Title: EE P.I.R (4/7)

Size: | Document Number: LA-F402P | Rev:

Date: Friday, August 17, 2018 | Sheet 66

Eletro-X

tfersion Change List (P. I. R. List)

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
39	47	Power control	2017/04/19	EE	EC request to reseve OR gate for WLAN power EN	Reserve DZ9 4/20 RZ38 PD change to WLAN_PWR_EN_UZ2	0.1(X00)
40	36	MEC5105 Support	2017/04/19	EE	EC request to reseve ESPI_RESET# for JESPI	Reserve RE560	0.1(X00)
41	All	All	2017/04/19	EE	OTG support	Pop RT74, Depop RC337 4/20 RC337 10K to GND	0.1(X00)
42	35	EC MEC5105	2017/04/19	EE	Dell request to add test point for EC free pins	Add test point T141 for UE1.D1>GPIO051 Add test point T142 for UE1.L11>GPIO054 Add test point T264 for UE1.F13>VBUS3_ECOK Add test point T143 for UE1.K7>GPIO011 Add test point T144 for UE1.M1>GPIO100 Add test point T262 for UE1.J6>GPIO202 Add test point T147 for UE1.M4>DGPU_PWROK only UMA	0.1(X00)
43	38	USH & TPM	2017/04/19	EE	JUSH1 add net name	1. Add net name at DZ8.1 .	0.1(X00)
44	37	USH & TPM	2017/04/21	EE	TPM change to NPCT650x	Change UZ12 to SA00008EL80 and related resistors	0.1(X00)
45	37	USH & TPM	2017/04/24	EE	BOM option by ¡§650@¡¨ or ¡§750@	1.The pop option for VHIO power: NPCT750: VHIO=+3.3V_RUN NPCT650: VHIO=+3.3V_ALW_PCH 2.The pop option for SLP_S0# connection: NPCT750: pop RZ112 (SLP_S0#=GPIO0) NPCT650: pop RZ363 (SLP_S0#=GPIO2) 3.RZ62 can be removed	0.1(X00)
46	9	CPU (4/14)	2017/04/24	EE	JUART1 remove	remvoe JUART1, RC434	0.1(X00)
47	11	CPU (6/14)	2017/04/24	EE	Schematic align	INTRUDER# PU change to +RTC_CELL_PCH	0.1(X00)
48	All	All	2017/04/24	EE	GPIO map change	GPIO013 net name change to DGPU_PWROK UPD1_ALERT#>UPD1_SMBINT# UPD1_SMBUS_ALERT#>UPD1_SMBINT#_R	0.1(X00)
49	28	USB 3.0 CONN TYPE C	2017/04/13	EE	Swap ESD diode pin for layout	DT39 & DT40 swap pin	0.1(X00)
50	11	CPU (6/14)	2017/04/19	EMI	EMI request	1. Add RC550 for KBLR U42 .	0.1(X00)
51	35	MEC5105 ESPI EC	2017/06/06	EE	GPIO map change	UPD2_ALERT#>UPD2_SMBINT#	0.2(X01)
52	47	Power control	2017/06/06	EE	Change netname align with SB	WLAN_PWR_EN_U2> WLAN_PWR_EN	0.2(X01)
53	16	MCP(11/14) PWRVCCGT	2017/06/06	EE	Add netname for layout	RC437.2 > +VCC_GT_K52 RC438.1 > +VCC_GT_AK52	0.2(X01)
54	35	MEC5105 ESPI Power control	2017/06/06	EE	EC request to reseve OR gate for WLAN power EN	Add QZ15 and RZ518 Change SIO_SLP_WLAN# to SLP_WLAN#_GATE (EC side UE1.K10) & Add RE552	0.2(X01)
55	26	[Type C]PD Controller TI1	2017/06/06	EE	PD ROM main source change	UT6 change to SA000095R10 (GD)	0.2(X01)
56	11	MCP(6/14) CLK,PM,RTC	2017/06/07	EE	Schematic align, avoid SUSACK#_R floating	Reserve RC551	0.2(X01)

Eletro-X Technical

DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.

Title: EE P.I.R (5/7)

Size: Document Number: LA-F402P

Date: Friday, August 17, 2018 Sheet 67

Eletro-X

tfersion Change List (P. I. R. List)

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
57	37	NuvotonTPM1.2	2017/06/07	EE	Nuvoton request to change TPM_PIRQ# power rail TPM change to NPCT750	TPM_PIRQ# power rail change to +3.3V_ALW_PCH Change UZ12 to SA0000AQ200 and related resisto rs	0.2(X01)
58	24	DP to VGA & VGA ConnRTD2166	2017/06/07	EE	RTD2166 question	UV6.12 add RV622 PU to +3.3V_RUN	0.2(X01)
59	28	[Type C]USB 3.0 CONN TYPEC1	2017/06/07	ESD	ESD request	DT10, DT13, DT14, DT17,DT18,DT5,DT6,DT9 change from SC40000AT00 to SC40000DF00	0.2(X01)
60	37	NuvotonTPM1.2	2017/06/07	EE	For RBOM request.	CZ75 from 4.7uF to 10uF	0.2(X01)
61	33	NGFF Card	2017/06/07	EE	Correct the symbol	Update JNGFF1/JNGFF2 symbols	0.2(X01)
62	20,36	All	2017/06/08	EE	Main source change	UD1, UE4, UE6 change to SA00007WE00	0.2(X01)
63	46	All	2017/06/08	DFB	DFB request	PCB hole from 3.2mm to 3.3mm Location:H34,H35 LA13 symbol change to " TAIT_HCB2012KF121T50_2P"	0.2(X01)
64	ALL	All	2017/06/12	DELL	Dell request to change cap to Lend P/N	Lend P/N for all cap	0.2(X01)
65	36	MEC5105 Support	2017/06/14	EE	BOARD_ID change	Change RE79 to 130Kohm? (rev. X01)	0.2(X01)
66	11	HDMI conn	2017/06/14	EE	Crystal Vendor suggest	CC21,CC22=12pF	0.2(X01)
67	12	MCP(7/14)MISC, JTAG,HDA,SDIO	2017/06/14	ESD	ESD request	Add CC336 100P, place near CPU side	0.2(X01)
68	34	DMIC	2017/06/14	RF	RF request	CA54 change to 27pf	0.2(X01)
69	41	All	2017/06/15	DELL	DELL request	11. pop PJP33 12. Nonpop UZ23,CZ129,CZ130,PJP32 21. del UZ37,CN50,CN51,PJP30	0.2(X01)
70	9	MCP(4/14)GSPI ,I2C,UART,ISH	2017/06/15	EE	GPIO map change	Add TypeC_CON_SEL1/TypeC_CON_SEL2 for UC1.W4/UC1.AB3 Reserve RC553RC556 for connector selection	0.2(X01)
71	47	Power Control	2017/06/15	EE	EC request to reseve OR gate for WLAN power EN	Change QZ15 to SB00000T000	0.2(X01)
72	47	DP/USB Redriver SW1 TUSB546	2017/06/15	EE	PS8743 colay	Add RT410, RT411, RT412,RT413, RT414, RT415, RT416,CT213 Add RT405, RT406, RT407, RT417, RT418	0.2(X01)
73	24	DP to VGA & VGA ConnRTD2166	2017/06/21	EE	RTK suggest	LV19/LV20 > RV650/RV651 §ï75£[; CV132/CV133 §i2P	0.2(X01)
74	26	[Type C]PD Controller TI1	2017/06/21	EE	TPS65982(UT5) update version	DB > DC (SA0000AX700)	0.2(X01)
75	34	Codec ALC3246	2017/07/26	ESD	ESD request	DA2, DA6, DA7 change main source from SCA00002900 to SCA00001A00	0.3(X02)
76	All	All	2017/08/01	EE	Change cap to 0end P/N	0end P/N for all cap	0.3(X02)
77	26	[Type C]PD Controller TI	2017/08/02	EE	TI TPS65982 request(TBTA_DEBUG4)	pop RT407 when pop 8743 & change to 10K	0.3(X02)
78	28	USB 3.0 CONN TYPE C	2017/08/02	EE	SE part COS issue.	CT99, CT100, CT101, CT102 change to 0.01u_X5R_0201_25V (SE00000YH00)	0.3(X02)

Eletro-X Technical

DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.

Title: EE P.I.R (6/8)

Size: Document Number: LA-F402P

Date: Friday, August 17, 2018 Sheet 68

Eletro-X

tfersion Change List (P. I. R. List)

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
79	25	DP/USB3 Repeater SW TUSB546	2017/08/02	EE	TI update version(TUSB546A)	TUSB546 change form SA00009R710 to SA00009R720	0.3(X02)
80	All	All	2017/08/03	EE	To avoid inrush current caused voltage drop	Add soft start solution(only reserved) on QV8,QZ1 (add CV635, CZ200, RZ380,RV400) 8/4 Add soft start solution(only reserved) on QE15,QC7 (add CC340,RE565)	0.3(X02)
81	All	All	2017/08/07	RF	RF request	1. pop C219,CC220,CC221,CC225,CC337,CV11,CV16,CZ62,CZ6,CZ64,CZ67,CZ68, CZ85,CZ86,CZ87,CZ91,CZ92 2.add LZ2,CZ210,CZ211,CE70,CZ212,LE1,CI50~CI52,CC341 3.del RZ85,RZ87	0.3(X02)
82	36	MEC5105 Support	2017/08/08	EE	BOARD_ID change	Change RE79 to 62Kohm? (rev. X02)	0.3(X02)
83	9	CPU (4/14)	2017/08/09	EE	TPM Pin connectivity requirement	Add RC560,RC561(reserved) BOM options.	0.3(X02)
84	All	All	2017/08/11	EE	Buyer request	main source change 1 .SC1N4148180 > SC100005500 2. SC100000S00 > SCS00003700	0.3(X02)
85	36	Board ID	2017/9/11	EE	Board ID change	RE79 change to (A00)4.3K = SD028430180	1.0(A00)
86	12	ME SW	2017/9/11	EE	ME SW depop	depop RC222,SW1 RC221 change to 0ohm short pad	1.0(A00)
87	ALL	0 ohm change to short pad	2017/9/11	EE	0 ohm change to short pad	RC294,RC295,RC296,RC328,RC422,RC550,RC444,RC445,RE32,RE290,RE548,RE552, RN99,RN186,RN187,RN192,RN223,RN224,RN225,RR5~RR10,RT54~RT57,RT74,RV323, RZ56,RZ61,RZ64,RZ89,RZ368,RZ112,RZ365	1.0(A00)
88	ALL	0 ohm change to short pad	2017/9/15	EE	Only support DS3 0 ohm change to short pad	RC439,RC441,RE536	1.0(A00)
89	37	change P/N	2017/9/15	EE	TPM change to MP sample	UZ12 change to SA0000AQ220	1.0(A00)
90	9	GPIO map change	2017/9/15	EE	GPIO map change	Drop win7 debug depop RC330, RC331	1.0(A00)
91	ALL	DFX request	2017/9/18	EE	Close solder mask	LV3,LV6,LV9,LV12 RI47,RI48,RI49,RI50, RI27,RI28,RI29,RI30 CMOS1,CI32	1.0(A00)
92	38	DFX request	2017/9/18	EE	Modify the DZ8 footprint	Modify the DZ8 footprint to follow DE2. because pcb pad is smaller	1.0(A00)
93	26	(Type C)PD Controller TI	2017/11/14	EE	component poor supply	CT74,CT83 change from SE00000OU00 to SE00000QL10	1.0(A00)
94	11 13 17 18 20 21 23 31 35 36	MLCC downsize	2018/04/18	EE	component poor supply	deletef°CC24 CC25 CC199 CC203 CC204 CC205 CC206 CC207 CC208 CC211 CC212 CC213 CC215 CC216 CC217 CC218 CC222 CC251 CC253 CC264 CC265 CC326 CD9 CD10 CD11 CD12 CD13 CD14 CD15 CD16 CD18 CD19 CD23 CD24 CD41 CD42 CD43 CD44 CD45 CD46 CD47 CD48 CD50 CD51 CD55 CD56 CE10 CE14 CE30 CE31 CE63 CR15 CR22 CZ100 CZ102 CZ105; add: CC78~CC81, CC84~CC113, CC118,CC119, CC122~CC129,CD108~CD111, CD64~CD107, CE101 CE102 CE141 CE142 CE301 CE302 CE311 CE312 CE631 CE632 CR1501 CR1502 CR2201 CR2202 CZ1000~CE1005	2.0(A01)

DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.

Title: EE P.I.R (7/8)

Size: Document Number: LA-F402P

Date: Friday, August 17, 2018 Sheet 69

Eletro-X Technical

tfersion Change List (P. I. R. List)

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
95	44	USB POWER	2018/04/18	EE	component poor supply	CI8/CI801 COLAY	2.0(A01)
96	36	Board ID	2018/04/18	EE	Board ID change	RE79 change to (A01)2K	2.0(A01)
97	18	improve ripple	2018/08/11	EE	WHEA BSOD issue	CC221,CC219,CC220,CC226 from 0805 47uf to 0603 22uf ; RC171 from 0402 0ohm to 0603 0ohm	3.0(A02)
98	36	EC MEC5105 Support	2018/08/17	EE	Board ID	Change RE79 to 240Kohm (rev. A02)	3.0(A02)

Eletro-X Technical

DELL CONFIDENTIAL/PROPRIETARY

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.

Title: EE P.I.R (8/8)

Size: Document Number: LA-F402P

Date: Friday, August 17, 2018 Sheet 70

Eletro-X